



## High Performance & Low Cost Flash Solution – Multi-I/O New Generation Serial Flash

NOR FLASH Memory is usually divided into Parallel Flash or Serial Flash with the distinction being the type of I/O interface used. Parallel flash uses parallel buses to transfer address and data information. And as its name implies, Serial Flash uses a serial bus to transfer that same address and data information. Serial flash typically uses the Serial Peripheral Interface (SPI) bus for command and data transfers. Traditionally, Parallel Flash has provided faster access speed and the ability to eXecute code In Place (XIP). The much more compact Serial Flash has been utilized to store data only or alternatively, download boot code to DRAM or SRAM. In this case the code gets executed out of the DRAM or SRAM. Although Serial Flash has advantages in terms of cost and lower pin counts, its significantly lower data throughput prohibits its deployment in many applications.

The next generation Multi-I/O Serial Flash offered by Macronix not only provides the cost advantage of Serial Peripheral Interface, but it also provides outstanding access time, which enables system designers to consider Serial Flash for speed critical applications. This article will elaborate and provide additional insights into this next generation Serial Flash.

### **Minimized System Efforts: Backward Compatibility, Same Footprint**

The Macronix Multi-I/O Serial Flash doubles or even quadruples the data rate by changing the conventional Serial Input pin and Serial Out pin from single unidirectional data flow into multiple bi-directional data flows. This doubling or quadrupling of data rate allows serial flash to compete with Parallel Flash in terms of data read performance. There is more good news: this high data read performance can be enjoyed with perfect backward compatibility with the device occupying the exact

same footprint used by conventional single I/O flash in 8-pin SOP packages. In other words, there is no need to modify the PCB or change the socket.

In the single I/O mode, pin 5 is used as the Serial Input (SI) – command and data are written into memory through this pin. In the Dual I/O mode, both the Serial Input (SI) pin 5 and Serial Out (SO) pin 2 are utilized as bidirectional pins (SI/SIO) as shown in Figure 1 below. Pin 5 is still used for writing the command but both these pins can be used to write the address. Data is then read from SI and SO. By changing these two pins from unidirectional to bi-directional pins and inputting address information and reading data two bits at a time, a 2-to-1 read speed advantage over single I/O operation is realized. Similarly, the Quad I/O Serial Flash expands on this concept by utilizing the Write Protect (WP#) pin and Hold (NC) pin as bi-directional pins in conjunction with the SI and SO pins to provide a total of four I/O pins and thus quadruples the effective data rate.

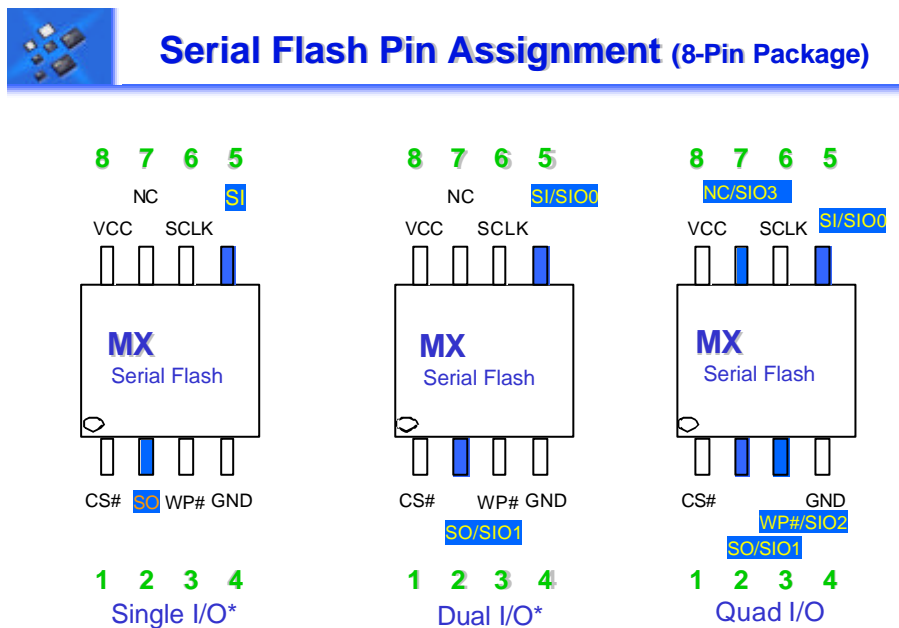


Figure 1. Macronix Multi-I/O Serial Flash Pin Assignments

**Current Serial Solution: Single I/O Serial Flash Read Speed Not Comparable with Parallel Flash**

From the viewpoint of a system designer, the 70ns read speed provided by Parallel

Flash is significantly faster than the standard 66 MHz read speed provided by Single I/O Serial Flash. This is clearly demonstrated by the simulations shown in Figure 2 below. Although Single I/O Serial Flash occupies much less board space, is easier to layout, and generates much less EMI and cross talk than a Parallel Flash device, the benchmark chart illustrates that it simply cannot compete with Parallel Flash in terms of data throughput.

Serial single I/O @ 66MHz				Parallel (x8) tAA=70ns	
overhead	command	8 clocks	=	606.061 ns	no overhead
	address	24 clocks			
	dummy	8 clocks			
		40 clocks			
data out	code length			data out time	
	1 byte	8 clocks , total		727 ns	1 byte 70 ns
	2 bytes	16 clocks , total		848 ns	2 bytes 140 ns
	3 bytes	24 clocks , total		970 ns	3 bytes 210 ns
	4 bytes	32 clocks , total		1091 ns	4 bytes 280 ns
	5 bytes	40 clocks , total		1212 ns	5 bytes 350 ns
	6 bytes	48 clocks , total		1333 ns	6 bytes 420 ns
	7 bytes	56 clocks , total		1455 ns	7 bytes 490 ns
	8 bytes	64 clocks , total		1576 ns	8 bytes 560 ns
	9 bytes	72 clocks , total		1697 ns	9 bytes 630 ns
	10 bytes	80 clocks , total		1818 ns	10 bytes 700 ns
		⋮			⋮
1M bytes	8,388,608 clocks , total		127,100,727 ns	1M bytes 73,400,320 ns	
	⋮			⋮	

Figure 2. The Readout Speed Comparison between Single I/O Serial Flash & Parallel Flash

### New Serial Solution: Multi-I/O Serial Flash Exceed Parallel Flash in Readout Speed

The Multi-I/O Serial readout speed performance can actually outperform Parallel Flash as shown in Figure 3 below because of the I/O functionality of the Multi I/O pins. By using the Quad I/O mode for example, when the code length of data or programming is longer than 4 bytes, the data-out speed of Serial Flash surpasses Parallel Flash.

## Enhanced Performance

When specifying addresses, traditional Single I/O Flash needs 40 clock cycles of overhead, of which 8 cycles are for re-writing the read command, 24 cycles for address allocation, and 8 dummy cycles. However, an added feature in the Multi-I/O Serial Flash offers Enhanced Performance by saving 20 clock cycles and further upgrades the performance. This new feature eliminates the need to repeat the 8 cycles used for commands when random addresses are being used. This feature is enabled whenever the system toggles all of the data bits between the first and second dummy cycles. In other words, the bits in the first dummy cycle should be the opposite of the bits in the second dummy cycle. This advises the device that the current command is to be repeated during the next operation. If this current operation is a Multi-I/O read command, the Flash will be kept in the Multi-I/O Read Mode and the next read operation can be initiated by simply supplying a new address and the required number of dummy cycles. This accelerates the read operation by eliminating 20 extra cycles compared to a Single I/O Flash.

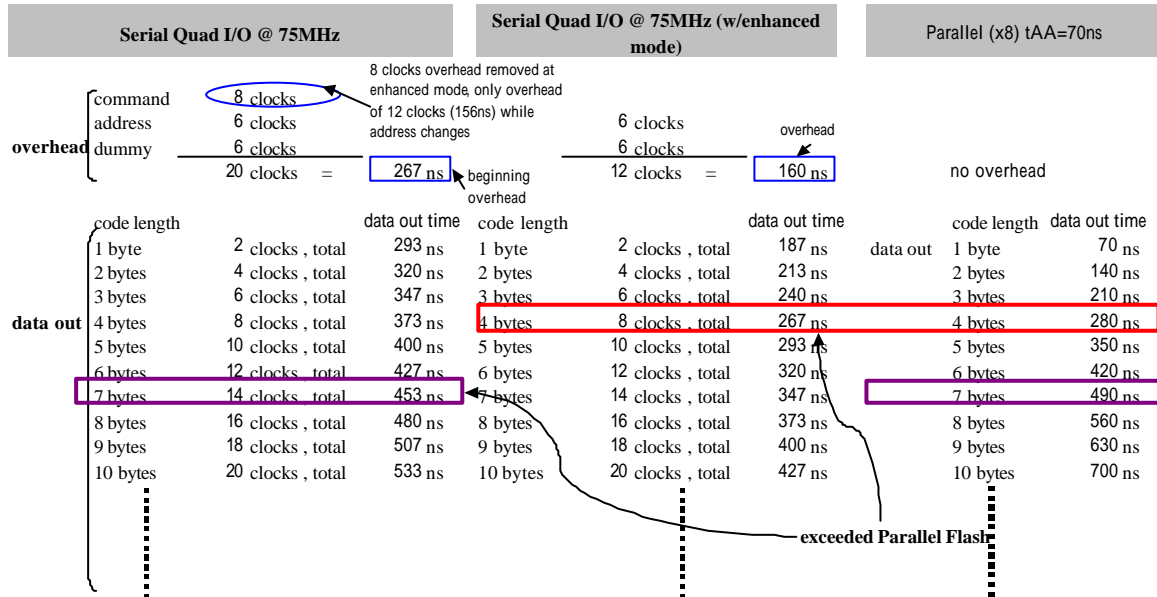


Figure 3. The Readout Speed Comparison between Multi-I/O Serial Flash & Parallel Flash

## Much Better Than Single-in/Multi-out Flash

There is another Serial Flash design that uses a single input only with multiple data

output pins. This approach is very different from the multi-in & multi-out approach discussed above. Rather than spread the input address bits over a number of pins, the single-in/multi-out approach requires all address bits to input through a single input pin serially with each address bit requiring one clock cycle. The multiple I/O approach allows up to four address bits to be input with each clock cycle. In addition to the quadruple speed improvement provided by quad input pins, the competing design does not provide the Enhanced Performance feature and could require an additional 26 cycles of overhead when random addresses are required during read operations. Besides the extra overhead clock cycles required by a single-in/multi-out approach, system designers must also consider the consequences of switching back and forth between a single input and multiple outputs. This is very inconvenient from a firmware point of view and would probably make XIP impractical. However, the multi-in & multi-out Flash approach is a much easier to deal with and will help facilitate XIP operations.

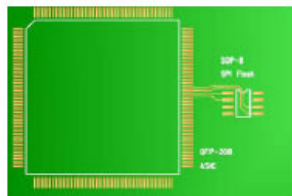
### **Serial Flash as the Cost Effective Solution**

From the whole system point of view, a system utilizing Serial Flash could massively reduce the I/O pin count for the Controller IC, which would also lower the cost of the IC itself. Furthermore, using Serial Flash significantly simplifies PCB layout, reduces board cost, and improves reliability (fewer interconnects). In terms of the number of control pins used by Parallel Flash, such as CE#, WE#, OE#, RD/BY#...etc, Serial Flash only needs two control pins (Clock and CS#). Moreover, Serial Flash requires at most 4 pins for I/O and address, replacing 38 external parallel interconnect lines by moving 16 data bus and 19 address bus lines inside of the chip. This simplification is another way to help save cost for system designers. This is clearly show in Figure 4 below.



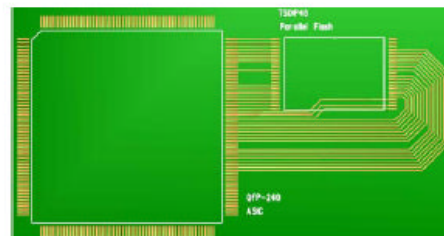
## Advantages of Serial Flash

- Simplifies PCB layout
- Reduces system noise, EMI
- Simplifies read interface
- Overall Flash + ASIC cost is reduced
- Lower power consumption compared to parallel flash



Layout with serial flash and controller

VS



Layout with parallel flash and controller

Figure 4. System Simplification Comparison between Serial Flash and Parallel Flash

To summarize, with Multi-I/O high performance along with cost savings with smaller packages, customers have been able to use these serial flash products in place of parallel flash for their XIP (Execute In Place) requirements. Several applications requiring high speed in PC servers, ODD as well as some newer communication applications are taking advantage of these higher speeds to offer end products with higher performance. Historically, Single I/O was quickly accepted and applied to a wide range of applications within 2 years of its time to market. It is therefore believed that Multi-I/O Serial Flash will soon take the lead again in the memory markets and become a major player in most applications.

Macronix International Co. Ltd, the second largest supplier of Serial Flash products in the industry, has devoted itself to work with major companies worldwide to develop new specifications of Serial Flash. With the mission to provide high performance and



cost effective solutions for all application needs, the Company is now introducing a new family of Multiple I/O Serial Flash products ranging from 16Mb to 64Mb densities in the smallest 8-pin and 16-pin packages in the industry. These cost-effective and highly reliable products are designed to be fully compatible to industry standard serial flash, along with enhanced features and flexibility not offered by other suppliers.