Macronix High Density Serial Flash Addressing

1. Introduction

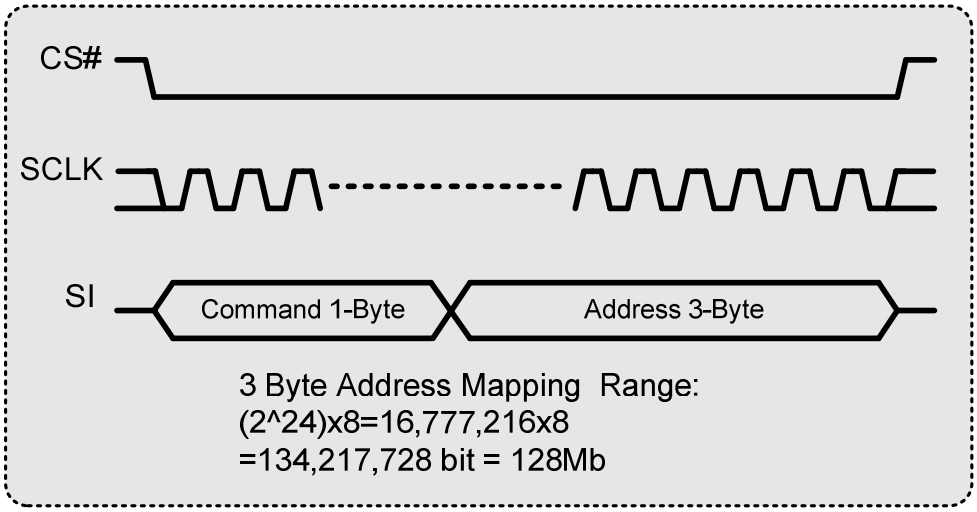
Many consumer products have converted or are converting from parallel flash to SPI serial flash. Generally, high end applications require higher memory density, but in the past, serial flash densities were limited to 128Mb due to addressing constraints. Macronix offers high density serial flash products with several different solutions to the previous 128Mb limitation. This application note will discuss the 128Mb addressing limitation and Macronix solutions to addressing 256Mb and above.

The information in this document is based on datasheets listed in Section 5. Newer versions of the datasheets may override the contents of this document.

2. 128Mb Memory Address Limitation

In general, the serial flash command protocol (Figure 2-1) uses a 1-Byte instruction opcode followed by a 3-Byte (24-bit) address. However, 3 bytes of address is only sufficient to define an address range of zero to 16MBytes (0 to 128Mb). In order to access flash above 128Mb, the address length needs to be extended to 4 bytes (32-bits) or use a 128Mb stacked die solution utilizing two CS# pins to select the top or bottom die.

Figure 2-1: 3-Byte Address Mapping Range



3. Macronix's Solutions to Access Memory ≥256Mb

Macronix provides products with several different solutions that enable full access to flash densities of 256Mb and larger. Table 3-1 shows access solutions and the 256Mb 3V products that support them. Please refer to the Macronix website for other densities and voltage options.

Table 3-1: Macronix 256Mb Product List

Access Solution	MX25L25635F MX25L25639F	MX25L25735F	MX25L25835E
Enter 4-Byte Address Mode	Yes	-	-
Extended Address Register (EAR)	Yes	-	-
4-Byte Address Command Set	Yes	-	-
Default 4-Byte Address Mode	-	Yes	-
Two CS# Pins (to control two stacked 128Mb flash)	-	-	Yes

3.1 Solution #1: Enter 4-Byte Address Mode

This solution requires the system to use an address-enhanced SPI protocol by adding a 4th address byte to all serial flash commands that normally use 3-Byte addresses. The device defaults to 3-Byte address mode, and 4-Byte mode is enabled with the EN4B command (0xB7). In 4-Byte mode, the legacy command set is still used*1, but 4-Bytes of address, instead of three, are sent during the address phase. The 4-Byte and 3-Byte address modes are mutually exclusive and only one can be active at a time. The EX4B command (0xE9) is used for exiting 4-Byte address mode. As shown in Figure 3-1, the device will also return to the default 3-Byte address mode after a power cycle, hardware reset, or software reset. The active address mode of the MX25L25635F and MX25L25639F can be determined by reading the Configuration Register and checking the "4BYTE" bit (Bit5 in Table 3-2). If it is set to '1', then 4-Byte address mode is active. Otherwise, 3-Byte address mode is active.

Note:
1. The number of address bytes in the following commands is independent of the 3-Byte and 4-Byte Address modes: 4READ for top 128Mb (0xEA), RDSFDP, RES and REMS.

Figure 3-1: 3-Byte Address to 4-Byte Address Flow of MX25L25635F

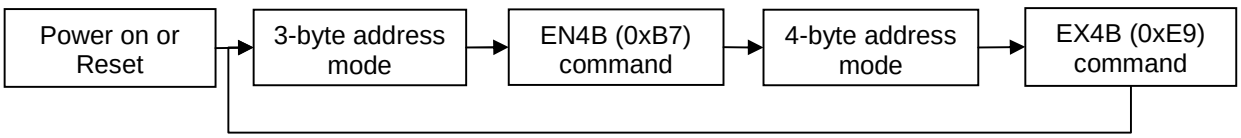


Table 3-2: Configuration Register (MX25L25635F and MX25L25639F)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DC1	DC0	4BYTE	Reserved	TB	OSD2	OSD1	OSD0
Dummy cycle		1=4-byte address mode (Default=0)		1=bottom area protect	Output driver strength		

3.2 Solution #2: Extended Address Register (EAR)

If the system only supports 3-Byte addressing, the Extended Address Register mode is an alternative method that can be used to access memory beyond the 128Mb limit. The device provides a volatile 8-bit EAR register that is automatically appended to the normal 3-Byte address and in effect creates a 4-Byte address[*1]. No commands are needed to enter or exit this mode. EAR mode operates with the legacy 3-Byte address command set.

As shown in Table 3-3, Bits[7:0] of the EAR correspond to address bits A[31:24] and must be loaded prior to its usage. The default value of the EAR is 0x00 and the standard 3-Byte address maps directly to the lower 128Mb of memory. An EAR value of 0x01 would remap a 3-Byte address into the upper 128Mb of memory. The usage model is as follows: system issues the Write Extended Address Register instruction (0xC5) with a register value used to set or clear EAR[0]. When cleared to '0', the bottom 128Mb memory can be accessed. When set to '1', the top 128Mb memory can be accessed. The system should check the EAR value before using it to access flash memory. This is done by using the Read Extended Address Register instruction (0xC8) and reading the 8-Bit EAR value.

The EAR supplies the higher address bits to form the starting address for read operations, but the EAR setting does not limit the read operation to the bottom or top 128Mb. For example, a read operation that begins in the lower 128Mb is free to continue reading into the upper 128Mb. Likewise a read operation that begins in the upper 128Mb is free to read to the end of memory and wrap around and continue reading into the lower 128Mb.

Note:
1. When device is commanded to enter 4-byte address mode, the EAR[7:0] becomes "Don't Care" for all commands using 4-Byte addresses.
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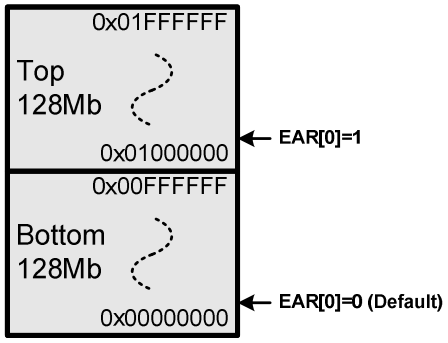
Table 3-3: Extend Address Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A31	A30	A29	A28	A27	A26	A25	A24
Reserved flash densities great than 256Mb →							256Mb
←							

Figure 3-2: Top and Bottom 128M bits



3.3 Solution #3: 4-Byte Address Command Set

This solution uses an alternate 4-Byte address command set (Table 3-4) that supplements the legacy 3-Byte address command set. Both command sets are always available and the system may choose which set to use. The operation of the 4-byte address command set is similar to the original 3-byte address command set with the only difference being 4-byte address commands require 4-Bytes of address (A31-A0) following the instruction opcode. The 4-Byte address command set eliminates the need to enter or exit 4-Byte addressing mode.

Table 3-4: 4 Byte Address Command Set

Command Set	READ4B	FASTREAD4B	2READ4B	DREAD4B	4READ4B	QREAD4B
Instruction Opcode	**13 (Hex)**	**0C (Hex)**	**BC (Hex)**	**3C (Hex)**	**EC (Hex)**	**6C (Hex)**
Address Bytes	4	4	4	4	4	4
Action	Normal Read	Single I/O Fast Read	Dual I/O Fast Read	Dual Output Fast Read	Quad I/O Fast Read	Quad Output Fast Read

Command Set	PP4B	4PP4B	BE4B	BE32K4B	SE4B
Instruction Opcode	**12 (Hex)**	**3E (Hex)**	**DC (Hex)**	**5C (Hex)**	**21 (Hex)**
Address Bytes	4	4	4	4	4
Action	Page Program	Quad Input Page Program	Block Erase (64KB)	Block Erase (32KB)	Sector Erase (4KB)

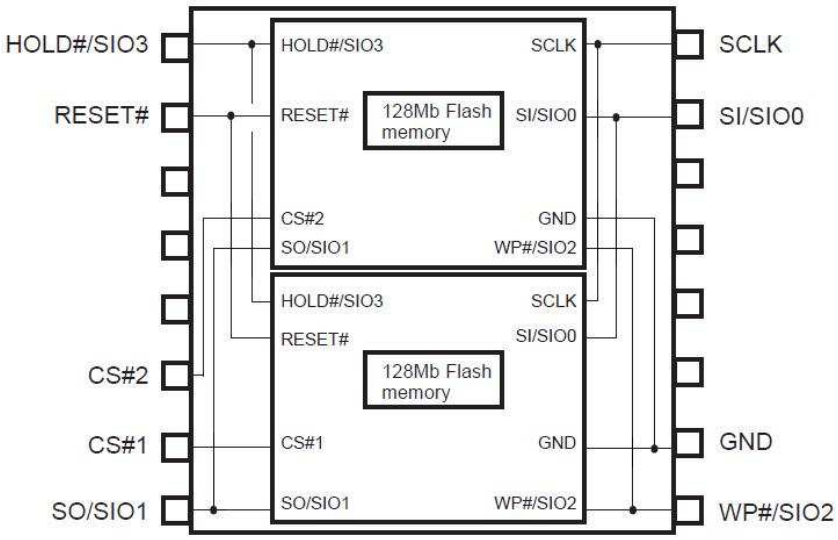
3.4 Solution #4: Default 4-byte Address mode

Macronix offers the MX25L25735F which defaults to 4-Byte address mode. The 4-Byte address mode is hardwired and no command or power cycle can change it to 3-Byte address mode. The MX25L25735F uses the legacy 3-Byte command set, but always requires 4-Bytes of address instead of 3-Bytes. The MX25L25735F does not use the 4-Byte address command set described in section 3.3.

3.5 Solution #5: 2x128Mb Devices Controlled By Two CS# Pins

The MX25L25835E is a 256Mb flash device built with two stacked 128Mb flash chips in the same package (shown in Figure 3-2). Two external CS# pins are used to select which of the two stacked die should be active. From the system's point of view, the device behaves like two independent 128Mb flash controlled by two independent CS# pins. It is up to the system to make sure that both CS#1 and CS#2 are not asserted simultaneously as a bus conflict will occur on the data lines. The MX25L25835E uses the legacy command set in 3-Byte address mode.

Figure 3-2: 2 CS# Pin Block Diagram



4. Summary

Macronix offers high density serial flash with a variety of solutions designed to solve the 128Mb address limitation. The user may refer to this application note to select a device appropriate for the addressing capabilities of their application.

5. Reference

Table 5-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please refer to the Macronix Website at http://www.macronix.com

Table 5-1: Datasheet Version

Data sheet	Location	Date Issue	Revision
MX25L25635F	Website	AUG. 07, 2012	Rev. 0.02
MX25L25639F	Website	SEP. 05, 2012	Rev. 0.01
MX25L25735F	Website	JUL. 18, 2012	Rev. 0.00
MX25L25835E	Website	NOV. 29, 2011	Rev. 1.0

6. Revision History

Revision	Description	Date
1.0	Initial Release	Dec. 17, 2012

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