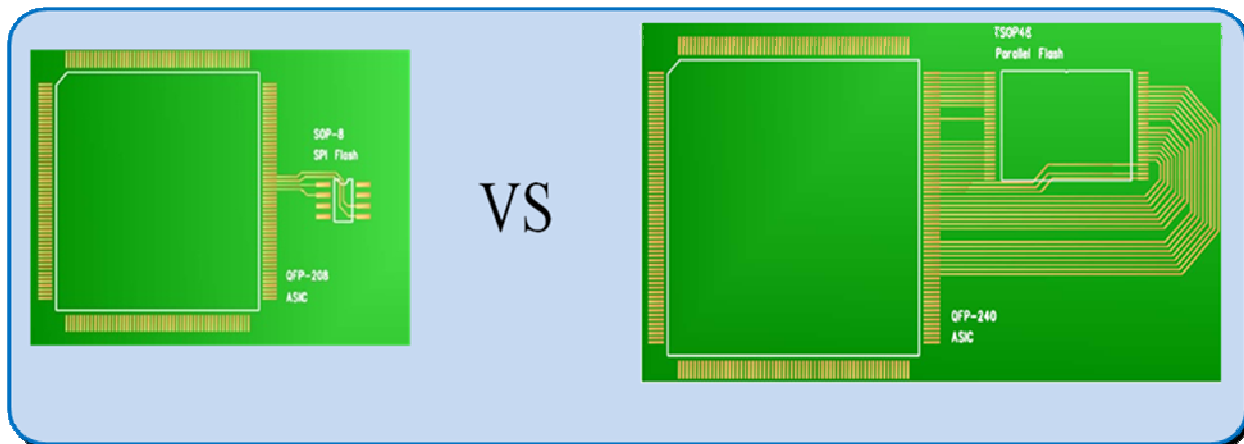


Macronix Serial Flash Multi-I/O Introduction

1. Introduction

All Macronix serial flash support a serial addressing protocol where 1 byte of instruction opcode is followed by a 3 byte (24 bit) address (note: may be a 4 byte address if the memory space is larger than 128Mb). Historically, to obtain faster data transfer rates and quicker system boot times, parallel flash were used as they had a parallel address bus and a parallel x16 data bus. Unfortunately, the wider busses resulted in flash package pin counts which ranged from 32 to 70 pins along with a similar increase in host interface pins, and an increase in PC board routing, all resulting in a higher BOM cost (Figure 1-1). To solve this problem, Macronix offers several serial flash families. For example, to increase performance, Macronix offers the MX25xxx35 series serial flash family (in both 1.8V and 3V densities ranging from 8Mb to 512Mb) in which commands, address, and data can be transmitted synchronously on as many as 4 channels in parallel. The serial interface can be configured in Single x1 I/O Mode (SPI), Dual x2 I/O Mode (DSPI), or Quad x4 I/O Mode (QSPI), with commands issued in either the SPI or QPI format. Not only do serial flash have performance similar to parallel flash when used in the x4 mode, but they are available in industry standard low pin count packages such as 8-SOP, 16-SOP and 8-WSON.

Figure 1-1: Serial NOR Flash vs. Parallel NOR Flash PCB Footprint



- **SPI flash has 4 signals (SCLK, CS, SI, SO) versus ~38 signals for Parallel NOR (19 address bus + 16 data bus + 3 control).**
- **Reduces EMI, system noise and power consumption.**
- **Aggregate bandwidth increases (similar performance).**
- **PCB area savings resulting in reduced BOM cost.**

This application note will clarify the differences between serial flash interface configurations and explain how to configure the flash in those modes.

Macronix Serial Flash Multi-I/O Introduction

2. Serial Flash Interfaces and Read Flow

Figure 2-1 shows how the Macronix serial flash communicates with the Host in SPI (Single I/O) mode. The flash synchronously receives the command, address, and data serially shifted in on one input pin SI (Serial In), and then the data is clocked out on SO (Serial Out). The entire sequence takes 48 clock cycles in FastREAD mode as shown in Figure 2-2.

Figure 2-1: Single I/O SPI Mode

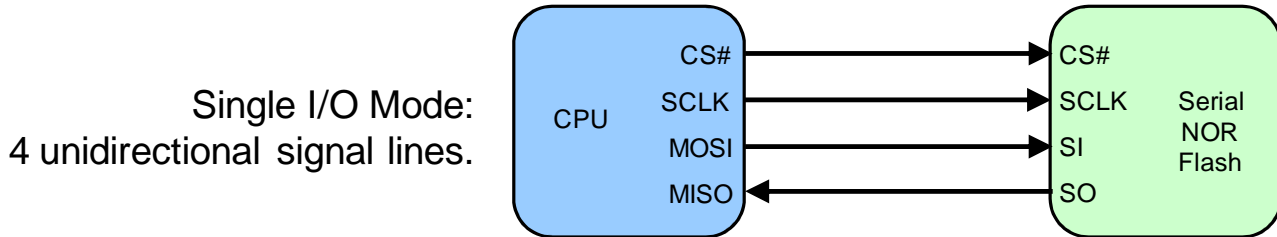
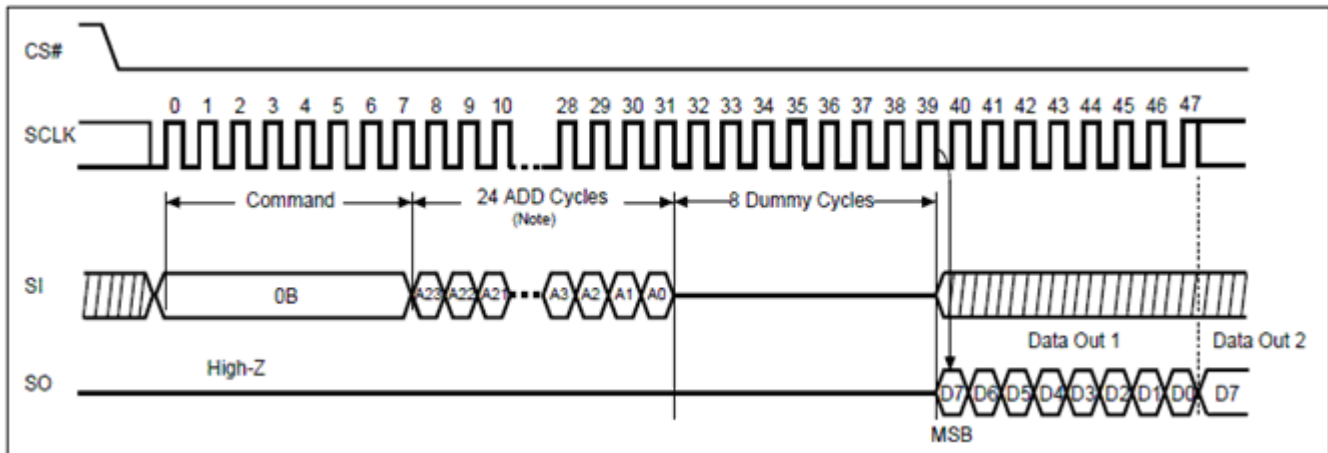


Figure 2-2: Fast Read (1-1-1) Timing Waveform



- Flash receives Commands on SI only.
- Flash receives Address on SI only.
- Flash sends Data on SO only.

Note: The address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Macronix Serial Flash Multi-I/O Introduction

Macronix Serial Flash provides Multi I/O functions by switching pin functions to support both a uni-directional and a bi-directional data bus. In SPI mode, the command is serial (single channel), but the number of channels used for address and data depends on the read command. A Dual I/O SPI mode uses SI and SO pins for data input and output, and a Quad I/O SPI mode (sometimes referred to as QSPI) uses SI, SO, WP#, and NC(or Hold#/Reset#) pins to serve as x4I/O data input and output. In QPI mode, commands, as well as address and data are sent in x4 mode.

In the x-y-z notation used in this applications note, x specifies the number of channels for the command, y specifies the number of channels for the address, and z is the number of channels for data.

Here is a description of the Macronix serial flash Read modes:

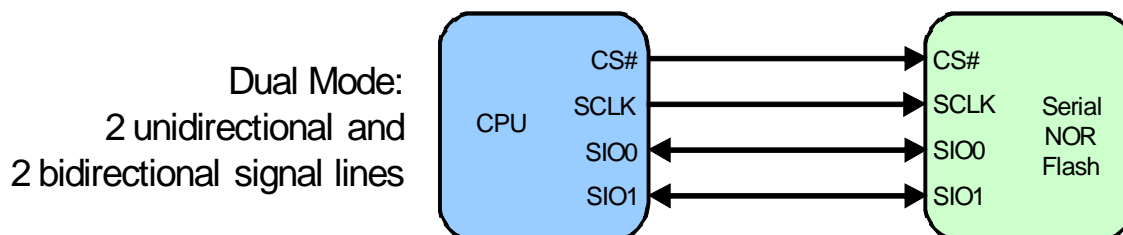
1. FastREAD (cmd = 0Bh): 1-1-1, Single I/O **SPI** Mode Read
 1-1-1 = cmd on 1 channel, address on 1 channel, data on 1 channel.
2. DREAD (cmd = 3Bh): 1-1-2, **DSPI** Mode Dual-Output Read
 1-1-2 = cmd on 1 channel, address on 1 channel, data on 2 channels.
 (see Figures 2-3 and 2-4)
3. 2READ (cmd = BBh): 1-2-2, **DSPI** Mode Dual-I/O Read
 1-2-2 = cmd on 1 channel, address on 2 channels, data on 2 channels.
 (see Figures 2-3 and 2-6)
4. QREAD (cmd = 6Bh): 1-1-4, **QSPI** Mode Quad-Output Read
 1-1-4 = cmd on 1 channel, address on 1 channel, data on 4 channels.
 (see Figures 2-8 and 2-9)
5. 4READ (cmd = EBh): 1-4-4, **QSPI** Mode Quad-I/O Read
 1-4-4 = cmd on 1 channel, address on 4 channels, data on 4 channels.
 (see Figures 2-8 and 2-11)

In QPI mode, the command is received by the flash in 4 parallel channels as well.

6. 4READ (cmd = EBh): 4-4-4, **QPI** Read
 4-4-4 = cmd on 4 channels, address on 4 channels, data on 4 channels.
 (see Figures 2-8 and 2-13)

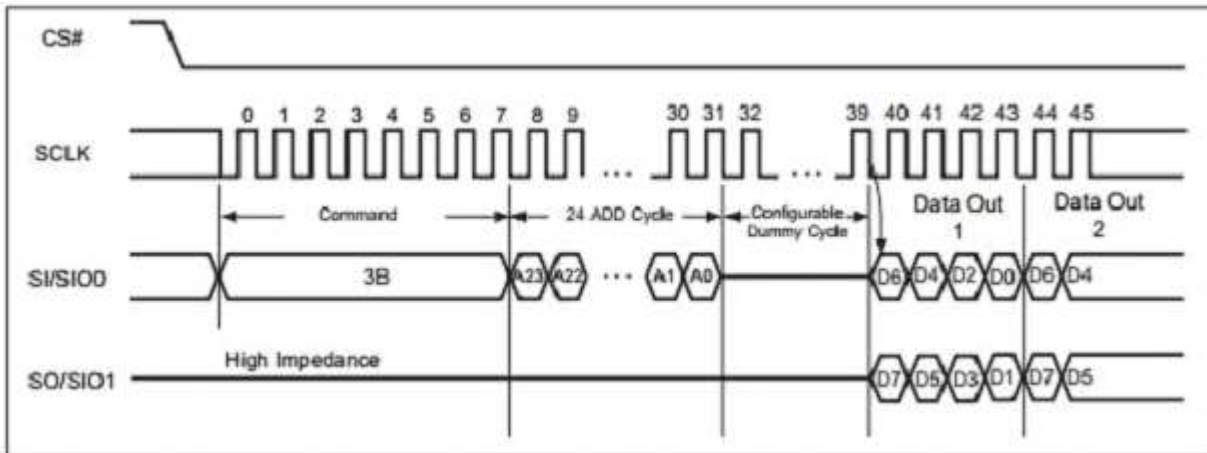
Notice that to read 1 byte of data from the flash in Serial x1 I/O (SPI) mode takes 48 clocks (Figure 2-2), 28 Clocks in x2 I/O DSPI mode (Figure 2-6). 22 Clocks in x4 I/O QSPI mode (Figure 2-11), and 16 clocks in x4 I/O QPI mode (Figure 2-13).

Figure 2-3: Dual I/O (DSPI) Mode



Macronix Serial Flash Multi-I/O Introduction

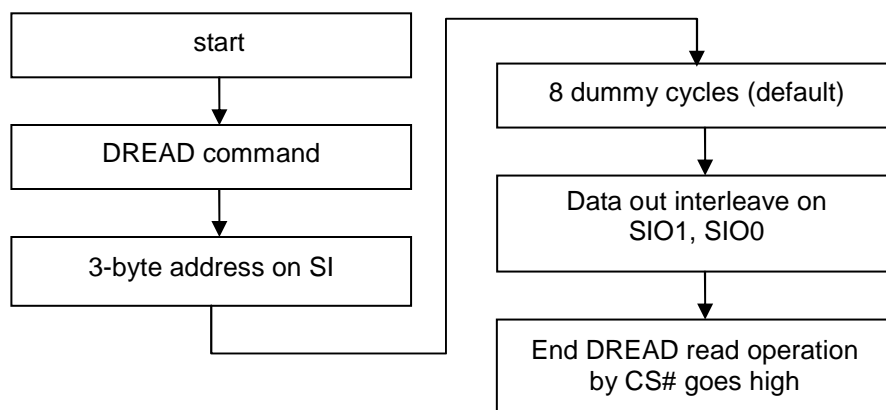
Figure 2-4: DSPI Mode, DREAD Timing Waveform [Dual Output Read = (1-1-2)]



- Flash receives Commands on SIO0 only.
- Flash receives Address on SIO0 only.
- Flash sends Data on SIO[1:0].

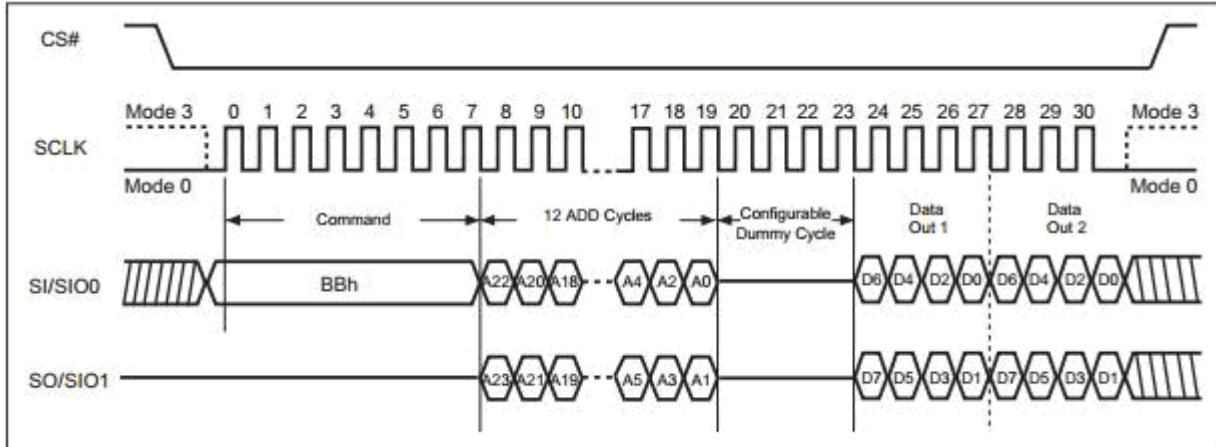
Note: the address cycles in Figure 2-4 are based on 3-byte address mode.

Figure 2-5: DSPI Mode, DREAD Flow [Dual Output Read = (1-1-2)]



Macronix Serial Flash Multi-I/O Introduction

Figure 2-6: DSPI Mode, 2READ Timing Waveform [2x I/O Read = (1-2-2)]



- Flash receives Commands on SIO0 only.
- Flash receives Address on SIO[1:0].
- Flash sends Data on SIO[1:0].

Note: The address cycles above are based on 3-byte address mode.

Figure 2-7: DSPI Mode, 2READ Flow [2x I/O Read = (1-2-2)]

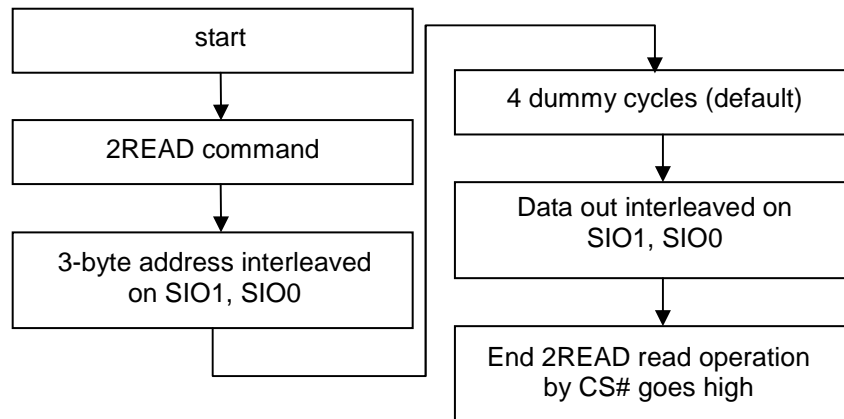
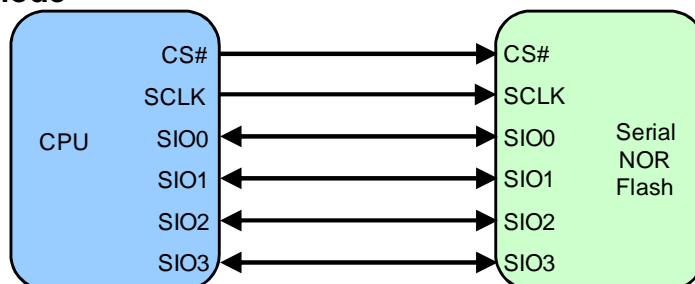


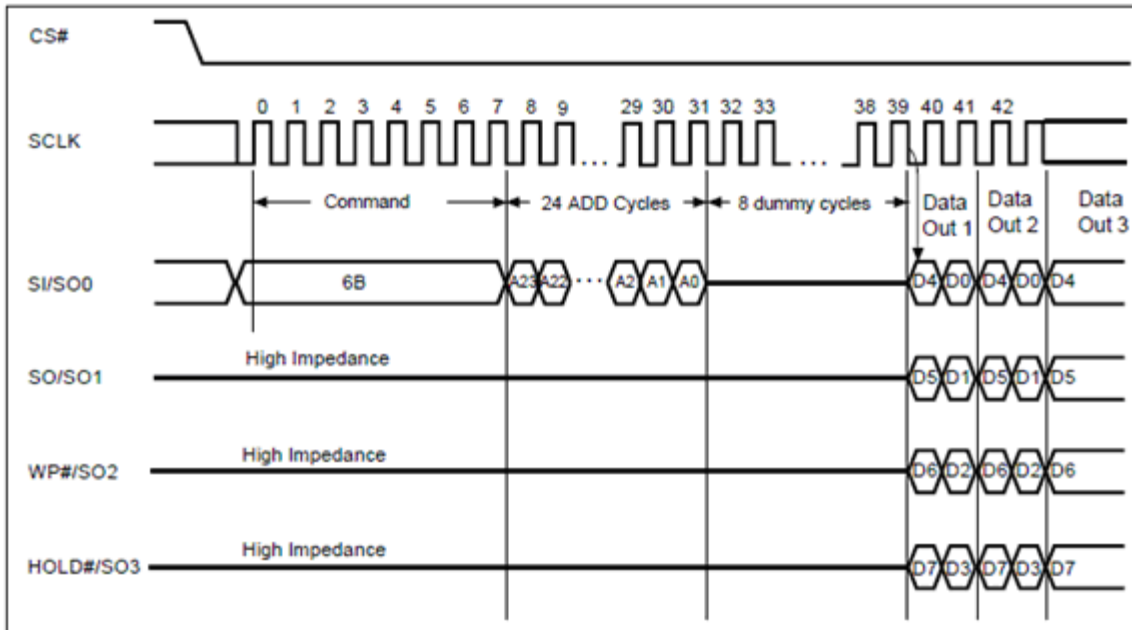
Figure 2-8: Quad I/O (QSPI) Mode

Quad Mode:
2 unidirectional and
4 bidirectional signal lines



Macronix Serial Flash Multi-I/O Introduction

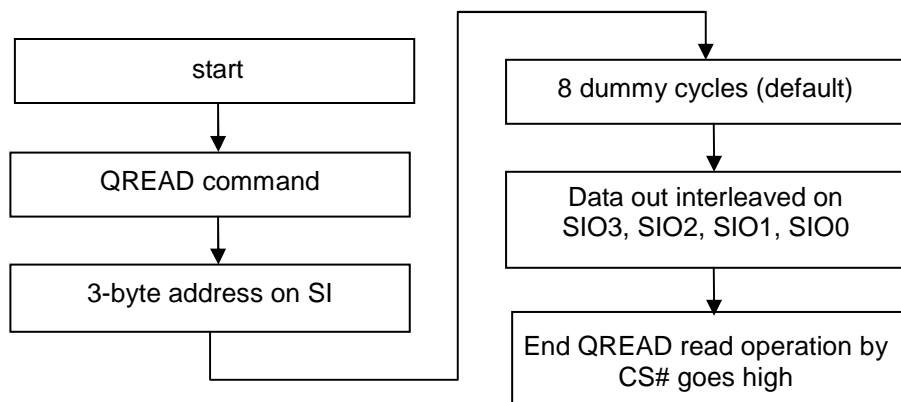
Figure 2-9: QSPI Mode, QREAD Timing Waveform [Quad Output Read = (1-1-4)]



- Flash receives Commands on SIO0 only.
- Flash receives Address on SIO0 only.
- Flash sends Data on SIO[3:0].

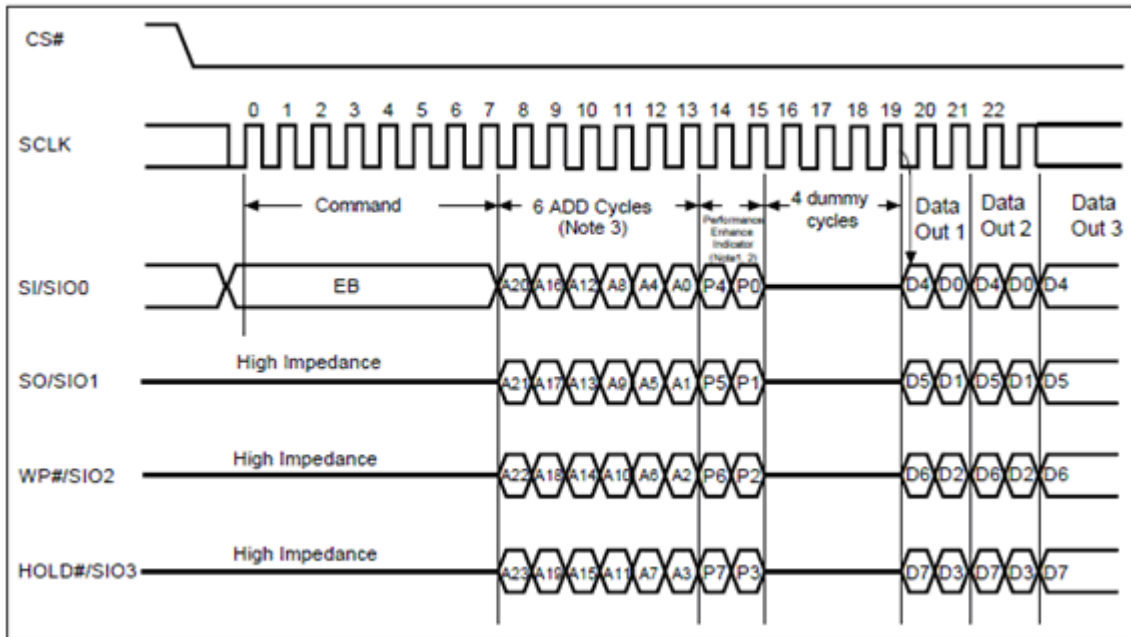
Note: The address cycles in Figure 2-9 are based on 3-byte address mode.

Figure 2-10: Figure 2-9: QSPI Mode, QREAD Flow [Quad Output Read = (1-1-4)]



Macronix Serial Flash Multi-I/O Introduction

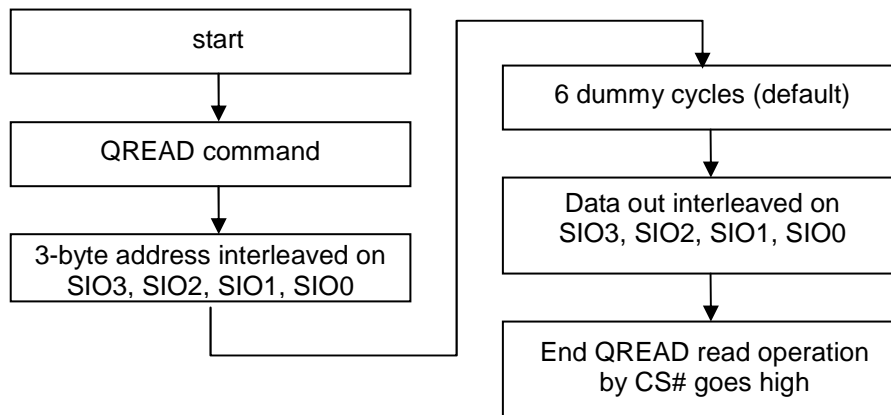
Figure 2-11: QSPI Mode, 4READ Timing Waveform [4 I/O Read = (1-4-4)]



- Flash receives Commands on SIO0 only.
- Flash receives Address on SIO[3:0].
- Flash sends Data on SIO[3:0].

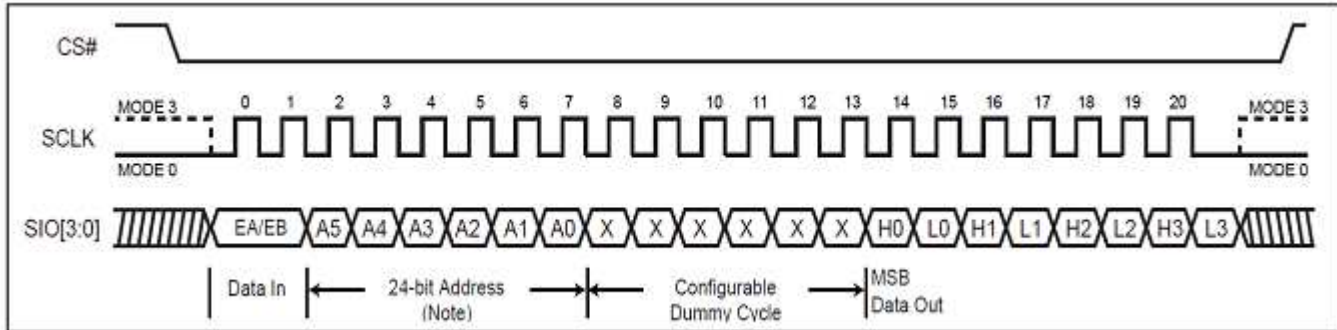
Note3: Please note the address cycles above are based on 3-byte address mode.

Figure 2-12: QSPI Mode, 4READ Flow [4 I/O Read = (1-4-4)]



Macronix Serial Flash Multi-I/O Introduction

Figure 2-13: QPI Mode, 4READ Timing Waveform [4 I/O Read = (4-4-4)]

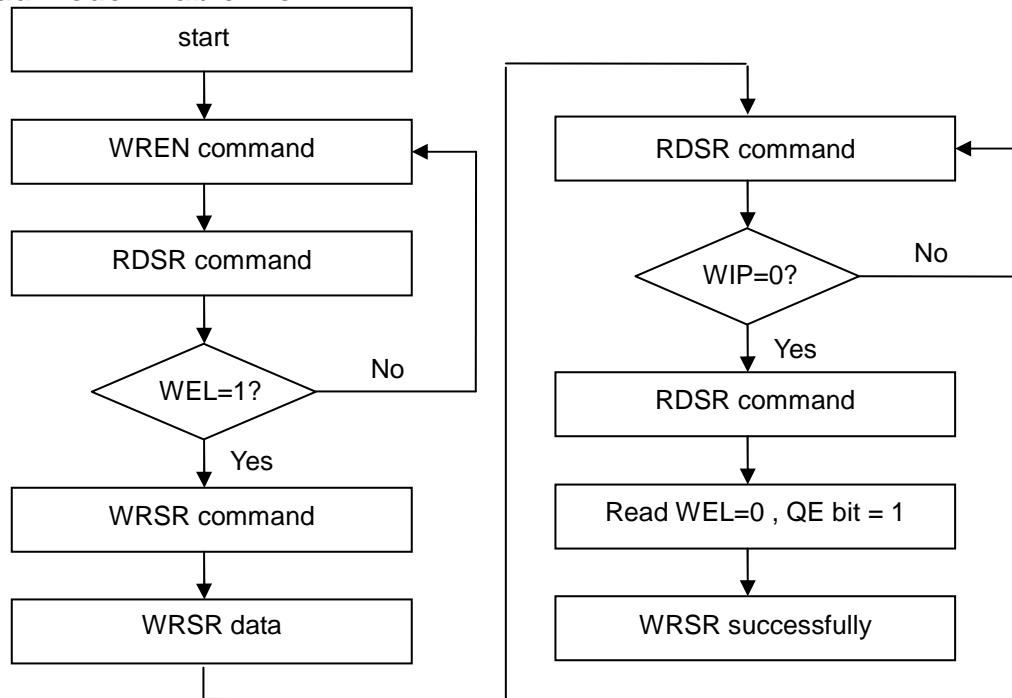


- Flash receives Commands on SIO[3:0].
- Flash receives Address on SIO[3:0].
- Flash sends Data on SIO[3:0].

3. Serial Flash Preparation for Quad I/O Operation

Macronix MX25xxx35 series serial flash is delivered in single I/O mode (x1 bus width). If however the Macronix serial flash will be used in Quad I/O mode (x4 bus width), the QE (Quad Enable) bit must be set to '1'. The non-volatile QE bit is Bit-6 of the Macronix serial flash Status Register. Figure 3-1 shows the flow used to set the QE bit, followed by a detailed description of the steps.

Figure 3-1: Quad Mode Enable Flow



Note: When QE bit is "1", it performs Quad I/O mode, and WP#, Hold#/Reset# are disabled.

Macronix Serial Flash Multi-I/O Introduction

The sequence to set QE is:

- 1) Send WREN (Write Enable) command (06h). This sets the WEL (Write Enable Latch) bit (Status Register bit 1).
- 2) Send WRSR (Write Status Register) command (01h) with 40h as the data. This sets the QE bit, but it takes some time for the WRSR operation to complete.
- 3) Use the RDSR (Read Status Register) command (05h) to poll the Status Register to check when bits 1 and 0 are clear. While the WRSR operation is still in progress, bits 1 and 0 will remain set to 1. Continue polling the status register until bits 1 and 0 clear to zero. Please refer to the product datasheet for additional details.

Note: the above steps are an overly simplified version of how to set the QE bit. Instead of simply writing 0x40 to the Status Register, the actual software may need to do a read-modify-write on the Status Register to preserve the state of the other non-volatile bits of the Status Register.

After the QE bit is set, all of the Fast Read (x1) commands are still supported along with the Quad Output (x4) Fast Read command. The Flash I/O pins "SIO2" and "SIO3" will tristate when not driving. The WP# and Reset/Hold# pin functions (if available) are now disabled.

The step to set the QE bit can be avoided if the Macronix MX25Lxx73 series serial flash is used, as the 73 series serial flash have the QE bit permanently set to '1'. At this time however, the 73 series is only available in 3V and in densities from 8Mb to 128Mb (Table 3-1).

For a desktop/notebook/PC Application, Macronix recommends the 73 series part as some chip sets check the SFDP (Serial Flash Discoverable Parameter) table 1st, and if Quad mode is supported, the chipset will begin talking in Quad mode. This problem is addressed with the 73 series part which has the QE bit permanently set to 1.

Macronix Serial Flash Multi-I/O Introduction

Table 3-1: Macronix Quad I/O Mode Serial Flash (32Mb to 512Mb)

Voltage	Density	Part Number
3V	32Mb	MX25L3235E
		MX25L3273E
	64Mb	MX25L6435E
		MX25L6473E
	128Mb	MX25L12835F
		MX25L12873F
256Mb	MX25L25635F	
512Mb	MX66L51235F	
1.8V	32Mb	MX25U3235F
	64Mb	MX25U6435F
	128Mb	MX25U12835F
	256Mb	MX25U25635F
	512Mb	MX66U51235F

4. Serial Flash Preparation for QPI Operation

In SPI (1-1-1) and QSPI (1-1-4 or 1-4-4) modes, the commands are always issued on one channel with 8 clocks. In QPI (4-4-4) mode however, commands are issued on 4 channels in 2 clock cycles (Figure 2-13).

The command EQIO (35h) is issued to enter QPI mode and is sent as a x1 serial stream. But once the serial flash receives this command and enters QPI mode, the serial flash expects subsequent commands, addresses, and data to be sent on 4 lines. There is no need to set the QE bit.

QPI is disabled with the RSTQIO command (F5h), software reset command, or a power cycle. Enabling QPI mode is different from setting QE=1. When QPI is enabled, Fast Read x1 (1-1-1) and Fast Read x4 modes 1-1-4 and 1-4-4 are not supported. When QPI is enabled (QE state is a "don't care"), only 4-4-4 mode is supported.

QE=1 and QPI are similar in the following manner:

When QE=1 or QPI is enabled, the "HOLD# /SIO3" pin functions as "SIO3" (the HOLD# feature is disabled) and the "WP#/SIO2" functions as "SIO2" (the WP# feature is disabled).

QE=1 and QPI are different in the following manner:

When QE=1 and QPI is not entered: Fast Read x1 (1-1-1), and Fast Read x4 (1-1-4 and 1-4-4) commands are all still supported.

Macronix Serial Flash Multi-I/O Introduction

5. Summary

Macronix serial flash read speeds can nearly double and quadruple when being used in x2 and x4 multi I/O modes.

Macronix offers different serial flash products with Multi-I/O interfaces, and these products are backward compatible to Single I/O serial flash offered by Macronix.

Macronix MX25xxxx35 series serial flash is delivered in single I/O mode (x1 bus width) by default. If single I/O mode or dual I/O will be used only, there is no need to set the QE bit. If however the Macronix serial flash will be used in Quad I/O mode (x4 bus width), the QE (Quad Enable) bit must be set to '1' or a Macronix 73 series serial flash that has QE preset to '1' should be used.

In SPI (1-1-1), DSPI (1-1-2 or 1-2-2) and QSPI (1-1-4 or 1-4-4) modes, the commands are always issued on one channel with 8 clocks. In QPI (4-4-4) mode however, commands are issued on 4 channels in 2 clock cycles. The command EQIO (35h) is issued to enter QPI mode. If the QPI mode has been entered, the QE bit does not need to be set.

6. References

Macronix Doc.	Description
AN0209	Macronix High Density Serial Flash Addressing

7. Revision History

Revision	Date	Description
01	July 25, 2013	Initial release



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INTERNATIONAL Co., LTD.

APPLICATION NOTE

Macronix Serial Flash Multi-I/O Introduction

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