Program/Erase Cycling Endurance and Data Retention in NOR Flash Memories

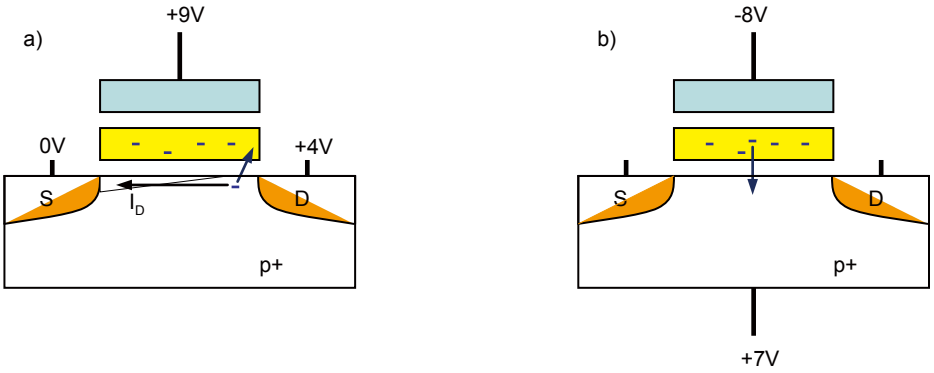
Introduction

NOR Flash memory cells are susceptible to degradation due to excessive Program/Erase (P/E) cycling. Worst case, if the number of P/E cycles exceeds the datasheet limit, the flash memory could fail, as the ability of the flash to retain information stored in the memory cells can be degraded over time. The relationship between Program/Erase cycles and data retention in NOR Flash memory will be discussed.

Flash NOR operation

Macronix NOR Flash memory design is based on floating gate Single-Level Cell (SLC) technology which has several advantages compared to other competing technologies. With floating gate technology, the programming operation is performed by means of Channel Hot Electrons (CHE) injection into the floating gate as shown in the *Figure 1(a)* and the erase operation is performed by extracting electrons from the floating gate through Fowler-Nordheim (FN) tunneling as shown in *Figure 1(b)*.

Figure 1. a) Floating-Gate Flash CHE Cell Program and b) FN-Tunnel Erase Mechanism



Note: Typical operation voltages are shown in Figure 1

Endurance and Retention

Cycling endurance can be defined as the capability of a flash memory device to continuously perform Program/Erase cycling to specification while the number of P/E cycles is within the specification limit. NOR Flash memories typically are specified to withstand 100K P/E cycles without suffering read/program/erase functional failures (please confirm with applicable flash datasheet).

Data retention can be defined as the capability of retaining stored information over time. Similarly, Data retention Time is the period of time the memory can retain data. Data retention time is a function of P/E cycles and temperature. Data retention time is typically specified to be a minimum of 20 years at 55°C for NOR Flash memories (please confirm with applicable flash datasheet).

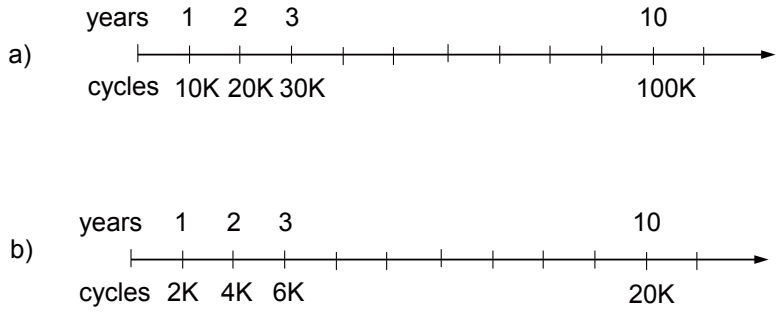
Due to the elevated electric fields normally used in the Program and/or Erase operations of flash memory cells, the tunnel oxide beneath the memory cell floating gates may become degraded over time. It is well known that charge traps may be created in the oxide leading to the reduction of endurance capability and data retention time.

The Flash memory is normally tested to the specification using industry standard reliability testing procedures [1,2,3,4]. Those testing procedures take into account the failure modes of modern flash technologies and typical application usage. For endurance testing, only a fraction of the memory array in each device is tested to the maximum specification otherwise the entire testing process would take too much time. For retention testing, a temperature acceleration model is used where the memory is baked at temperatures as high as 125°C and then the results are fit to confirm data retention time at system temperatures.

Reliability testing procedures are done in such a way as to consider the real application usage and the technology failure modes. For example, the standard procedure for testing endurance and retention will insert delays in between cycles because it is known that some oxide damage may be recovered, at least partially in between cycles. In typical real-life applications, erase cycles are distributed evenly across the memory array over the life of the application, instead of being concentrated in only the early stages. If the application has a different cycling rate, such as heavy cycling in a short time at the beginning of use, then the qualification procedure may not accurately model the usage. Special knowledge-based testing procedures must be used.

"Figure 2. Cycling Distribution over Device Lifetime" shows how normally P/E cycling is spread in time, in standard applications. For example, in *Figure 2 (a)* the application will reach 100K P/E cycles at end of life set in 10 years by erasing sectors about every hour. In case *(b)* the application is expected to reach 20K P/E cycles after 10 years erasing sectors about every four hours. The cycles are uniformly spread during the lifetime.

Figure 2. Cycling Distribution over Device Lifetime



It is useful to distinguish the Flash memory usage between uncycled and cycled conditions.

Data retention time for cycled devices decreases as the amount of P/E cycling count increases. It also follows that as the amount of P/E cycling increases, the time between P/E cycles (or the length of time the memory must retain the data) is also reduced. Using *"Figure 2. Cycling Distribution over Device Lifetime"* as an example, the time between cycles is four hours for case *(b)* and less than one hour for case *(a)*.

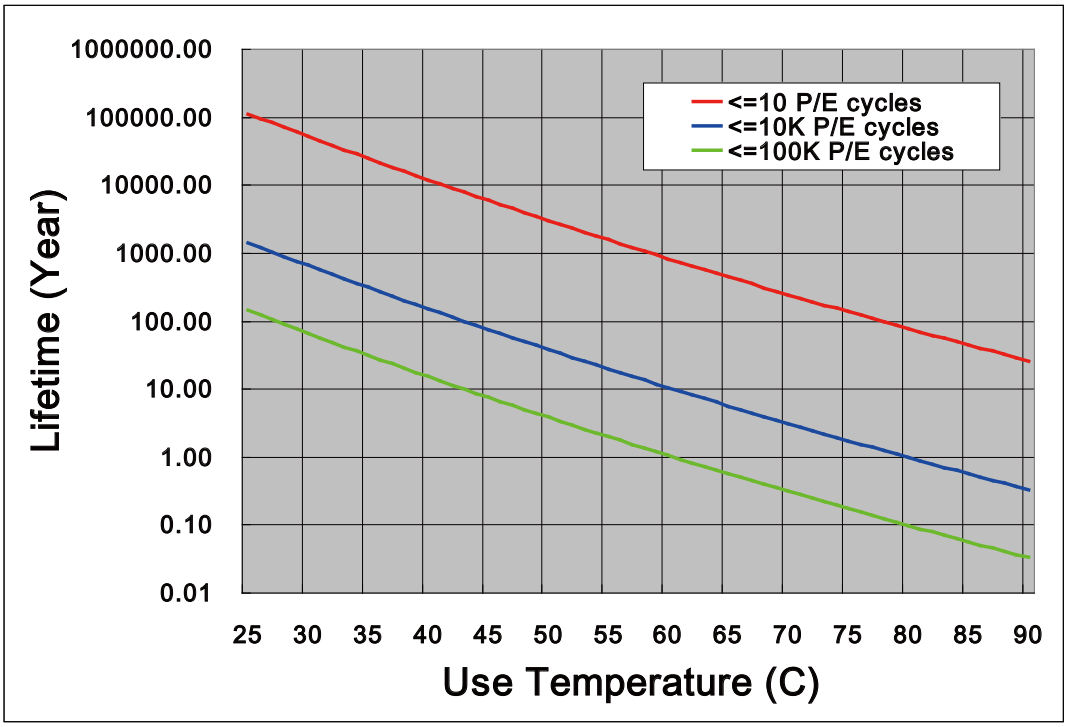
In some cases, only code data is stored in Flash memory and updates are rare. In other cases, information such as parameters or data captured are stored and they need be refreshed frequently. As a result, certain sectors may accumulate erase cycles very fast. In order not to exceed the maximum cycling limits during the lifetime it may be necessary to spread the data over multiple sectors. In order to have more reliable operation, wear leveling techniques should be implemented.

In cases when the system is not expected to be in use for long periods of time, and the data must be retained, it might be necessary to consider the cycling degradation effect on retention in order to meet the required retention time (especially under high temperature conditions). As an extreme example, let's consider a system such as the one in *Figure 2 (a)* where, after 100K cycles, the system is still expected to retain the data for years.

"Figure 3. Data Retention Lifetime after various P/E Cycles at T>= 55˚C" shows the relationship between retention and temperature for Macronix Flash. The various curves also illustrate the retention as a function of the erase cycles.

To obtain precise evaluations it is necessary to consider proper temperature usage profile instead of the maximum temperature reached by the application.

Figure 3. Data Retention Lifetime after various P/E Cycles at T>= 55˚C



Endurance and Retention Application Examples

Consider an application requiring updates of parameters such that a single memory block is filled-up every hour for ten years. One sector will reach 87K cycles at the end of the 10 year period if no wear leveling is used. Because the time between cycles is 1 hour, the retention capability is more than sufficient to maintain the data during the time period at the maximum temperature of 85°C as can be approximated using the bottom green curve in *"Figure 3. Data Retention Lifetime after various P/E Cycles at T>= 55˚C"*. In the case where the application ceases to be in use for a while, the device will still be able to retain the data for 20 years at roughly 35°C or two years at a constant storage temperature of 55°C.

The JEDEC standard JESD47 (Stress Test Driven Reliability Qualification of Silicon Devices) describes the general usage relation between Program/Erase cycling and data retention. In general, as the number of P/E cycles is increased, the data retention lifetime drops. In addition, if the interval between each P/E cycle is lengthened, the data retention capability can be increased.

In the case where an application requires the information be stored for a long time at a high temperature after cycling, it might be necessary to consider wear leveling, or other redundancy methods to maintain the consistency of the data. For a more accurate evaluation of the flash memory retention it is better to consider a temperature usage profile, instead of a worst case one, such as the one we previously mentioned where all of the cycling is done in the beginning of use.

To improve reliability, wear leveling is used to preventing certain memory blocks from reaching a high P/E cycling count, while other blocks are subjected to relatively few P/E cycles. At the highest level, wear leveling implementations consider a pool of blocks and program new data into the blocks that have been subjected to the least amount of P/E cycling. Each time, data is stored into different blocks, in order to reduce the erase cycle count per block.

The simple recommended example of wear leveling is to alternate the storing of parameters between two sectors/blocks in such a way that when the first sector is full the other one will be used. The full sector is meanwhile erased and made available again. This approach will automatically extend the cycling count as the number of erase cycles per sector are cut by half. Additionally, this approach is highly recommended in order to avoid losing data in the event of an unexpected power loss.

Another method which can be used to guarantee the appropriate retention time is to refresh the data blocks after a defined time. To employ such a technique it is necessary to have a timestamp available in the system. In addition to the techniques mentioned above, Error Correction Code (ECC) could be employed in the system to improve reliability.

Summary

NOR Flash memories offer high endurance and data retention capabilities in typical applications. However, for special applications, it might be necessary to implement special design techniques such as the use of wear leveling, data refresh, or ECC in order to achieve the required data retention.

References

1. JESD47I - Stress-Test-Driven Qualification of Integrated Circuits – JEDEC Standard.
2. JESD22-A117C - Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test – JEDEC Standard.
3. JESD94A - Application Specific Qualification Using Knowledge Based Test Methodology – JEDEC Standard.
4. JEP122D – Failure Mechanism and Models for Semiconductor Devices – JEDEC Standard

Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release	ALL	20th, Mar., 2014
REV. 2	Content modification	ALL	12th, Jun., 2014

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