Program/Erase Cycling Endurance and Data Retention of Macronix SLC NAND Flash Memories

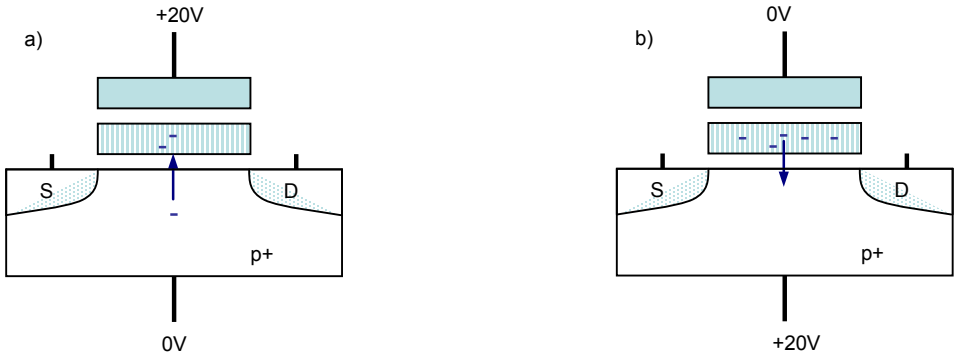
Introduction

NAND Flash memory cells are susceptible to degradation due to excessive Program/Erase (P/E) cycling. In the worst case, if the number of P/E cycles exceeds the datasheet limit, the Flash memory may not work normally. The ability of the Flash memory cells to retain stored information can also be degraded over time. This technical note will attempt to explain the relationship between the number of Program/Erase cycles and Data Retention time in SLC NAND Flash memory.

NAND Flash Memory Cell Operation

Macronix SLC NAND Flash memory is based on floating gate Single-level cell (SLC) technology which has several advantages compared to other competing technologies. With floating gate technology, NAND Program and Erase operations are performed by means of FN-tunneling to add or remove electrons from the Floating Gate as shown in *"Figure 1. Floating-gate FN-tunnel NAND Flash Program (a) and Erase (b) Mechanism"*.

Figure 1. Floating-gate FN-tunnel NAND Flash Program (a) and Erase (b) Mechanism



Note: The cell bias voltages shown in Figure 1 are typical and are for example purposes only.

Cycling Endurance and Data Retention

Cycling Endurance is defined as the capability of a Flash memory device to perform to specification if the number of P/E cycles is within the specification limit. Macronix SLC NAND Flash memories are specified to withstand typical 100K P/E Cycles without suffering Read/Program/Erase failures (please confirm with the applicable datasheet). Additionally, in NAND Flash, it is allowable that a certain number of blocks become bad (show failures) during the device lifetime. These blocks will be retired by proper Bad Block Management Ref.[1,2] without any impact on the application and will not be counted as endurance failures[4].

Data Retention is the capability of retaining stored information over time. The Data Retention Time is the period of time the memory can “retain” data in an unbiased condition. Also, data retention time is a function of P/E cycles and temperature. In general, data retention time is specified to be 10 years for NAND Flash memories (please confirm with applicable datasheet).

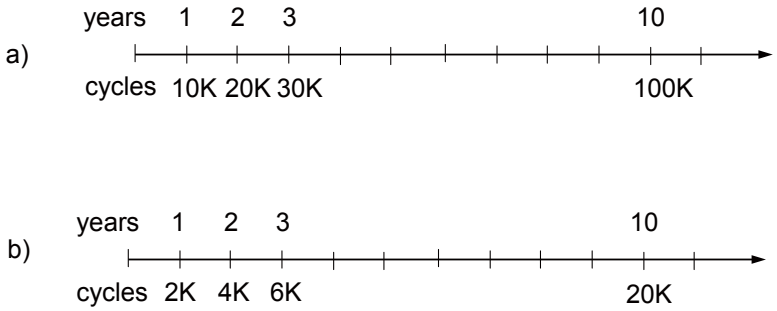
Because of the high electric fields normally used in Flash memory Program and Erase operations; the dielectric layers around the floating gate in the cell may suffer degradation over time as the number of P/E cycles increases. This is especially true for the tunnel oxide beneath the floating gate. It is well known that charge traps may be created in the oxide leading to the reduction of endurance capability and data retention time.

The Flash memory is normally tested to comply with the specification using industry standard reliability testing procedures[3,4,5,6]. These testing procedures take into account the failure modes of existing flash technologies and typical application usage. For endurance testing, only a fraction of the memory array in each device is tested to the maximum specification, otherwise the entire testing process would take too much time. For retention testing, a temperature acceleration model is used where the memory is baked at temperatures as high as 125°C and the results are fit to confirm data retention time at system temperatures.

Reliability testing procedures are done in such a way as to consider the real application usage and the technology failure modes. For example, the standard procedure for testing endurance and retention will insert delays in between cycles because it is known that some oxide damage may be partially recovered in between cycles. In the typical application usage, Erase cycles are spread over the whole life of the application, instead of being concentrated in the early stage. If the application has a different cycling rate, such as heavy cycling in a short time at the beginning, then the stress test procedure may not be accurate to model the usage. Special knowledge-based testing procedures must be used.

"Figure 2. Cycling Distribution over Flash Lifetime" shows how normally, P/E cycling is spread over time in standard applications. For example, in *"Figure 2. Cycling Distribution over Flash Lifetime" a)* the application will reach 100K P/E cycles at the end of its life in 10 years by erasing blocks about every hour, and in case *b)* the application is expected to reach 20K P/E cycles after 10 years by erasing blocks about every four hours. The cycles are uniformly spread during the lifetime.

Figure 2. Cycling Distribution over Flash Lifetime



It is useful to distinguish the Flash memory usage between un-cycled and cycled conditions.

Data retention time for cycled devices decreases as the P/E cycle number is increased.

It also follows that as the amount of P/E cycling increases, the time between P/E cycles (or the length of time the memory must retain the data) is also reduced. Using *"Figure 2. Cycling Distribution over Flash Lifetime"* as an example, the time between cycles is four hours for case *b)* and less than one hour for case *a)*.

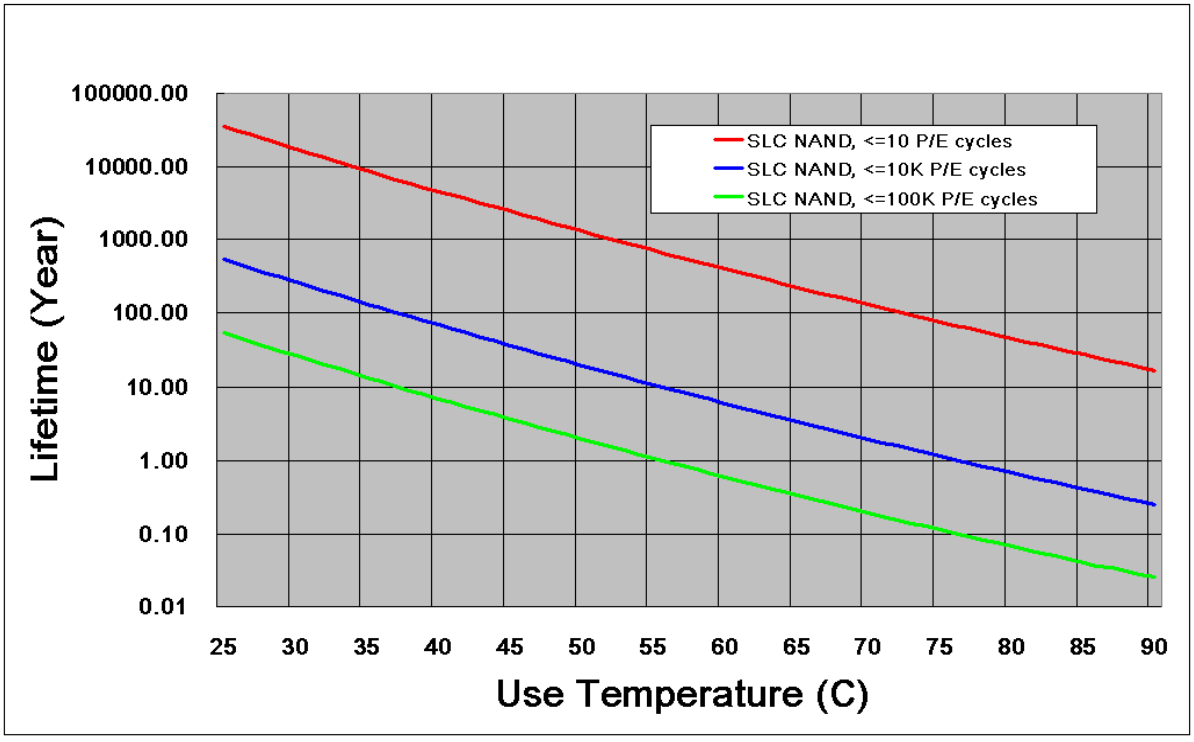
In some cases, only code data is stored in Flash memory and updates are rare. In other cases, information such as parameters or data captured need to be refreshed frequently. As a result, certain blocks may accumulate Erase cycles very fast. In order not to exceed the maximum cycling limits during the lifetime, it is suggested to spread the data over multiple blocks by implementing wear leveling techniques[2].

In the case when a system is not expected to be in use for long periods of time, and data must be retained during such a period, it might be necessary to consider the cycling degradation effect on retention in order to meet the required retention time (especially under high temperature conditions).

Figure 3 shows a typical relationship example between retention and temperature for Macronix SLC NAND Flash according to JEDEC JESD22-A117[4]. The various curves also illustrate the retention as a function of the erase cycles. The maximum retention specified for SLC NAND Flash is 10 years (Please check the actual datasheet). Lifetime is achieved by using the appropriate Error Correction (ECC) level defined in the datasheet.

To obtain precise evaluations, it is necessary to consider a proper temperature usage profile, instead of the maximum temperature reached by the application.

Figure 3. Example SLC NAND Intrinsic Retention Lifetime after P/E Cycling



Note: Typical Retention Lifetime is 10 years in SLC NAND Products.

Cycling Endurance and Data Retention Application Examples

As an example, let's consider an application requiring updates of parameters, such that a single memory block is updated every hour for ten years. One block will reach 87K cycles at the end of the 10 year period if no wear leveling is used. Because the time between cycles is 1 hour the retention capability is sufficient to maintain the data during the time period at the maximum temperature of 85°C as can be approximated by using the bottom green curve in *"Figure 3. Example SLC NAND Intrinsic Retention Lifetime after P/E Cycling"*. In the case where the application is not used for a while, the device will still be able to retain the data for 10 years at an ambient temperature of less than 35°C, or one year at 55°C.

Another example is the frequent data logging of parameters. We can imagine the need to store data (up to 2KB) every minute. Data will be written page by page, and each time a new page is written, the older one is made invalid by programming a specific marker. Since each block is composed of 64 2KB-pages, it means that a block will be filled in 64 minutes! Also in this case the block will be cycled about 82K times in 10 years. A savvy implementation will reserve eight blocks for data storage, thus reducing the cycling amount per block to 10K in 10 years. After 10 years and 10K of cycling per block the parameters can still be retained for one year in the harsh conditions of 75°C. Moreover, in this example the retention between cycles is not an issue because the parameters are being updated every minute. However, if the data logging is put into pause for a while, the retention condition can be satisfied easily.

The JEDEC standard JESD47 (Stress Test Driven Reliability Qualification of Integrated Circuits) describes the general usage relation between Program/Erase cycling and data retention. In general, as the number of P/E cycles is increased, the data retention lifetime drops. In addition, if the interval between each P/E cycle is lengthened, the data retention capability can be increased.

In cases where an application requires information to be stored for a long time at high temperature after cycling, it is recommended to consider wear leveling, or other redundancy methods to maintain the consistency of the data. For a more accurate evaluation of the flash memory retention, it is better to consider a temperature usage profile instead of a worst case one.

To improve reliability, generally wear leveling techniques[2] are used to prevent certain memory blocks from reaching a high P/E cycle count while other blocks experience relatively few P/E cycles. Wear leveling implementations consider a pool of blocks and program new data to the blocks with the lowest P/E count. Each time data is stored into different blocks in order to reduce the erase cycle count per block.

A simple example of a wear leveling implementation is to alternate the storing of data parameters into several blocks in such a way that when one block is full, a different one will be used. The previously used block is meanwhile erased and made available again. This approach will automatically extend the cycling count as the number of erase cycles per block are cut by the number of blocks used. Additionally, this approach may help to avoid losing data in the event of an unexpected power loss.

Another method which can be used to guarantee the appropriate retention time is to refresh the data blocks after a pre-defined time. To employ such a technique, it is necessary to have a timestamp available in the system to determine when a refresh is performed.

Lastly, in addition to the techniques mentioned above, ECC with correction capability greater than what is specified in the NAND Flash datasheet could be deployed in the system to improve reliability.

Summary

SLC NAND Flash memories offer high endurance and data retention capabilities in most applications. However, for special applications it might be necessary to implement special design techniques such as wear leveling, data refresh, and stronger ECC in order to achieve the required data retention.

References

1. Macronix Technical Note AN-0278 “Bad Block Information”
2. Macronix Technical Note AN0269 “Introduction to NAND in Embedded Systems”
3. JESD47I – “Stress-Test-Driven Qualification of Integrated Circuits” – JEDEC Standard.
4. JESD22-A117C – “Electrically Erasable Programmable ROM (EEPROM) Program/Erase Endurance and Data Retention Stress Test” – JEDEC Standard.
5. JESD94A – “Application Specific Qualification Using Knowledge Based Test Methodology” – JEDEC Standard.
6. JEP122G – “Failure Mechanism and Models for Semiconductor Devices” – JEDEC Standard

Revision History

Revision No.	Description	Page	Date
REV. 1	Initial Release	ALL	15th, Oct., 2014

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