# Comparing Spansion® S34ML04G200 with Macronix MX30LF4G18AC

## 1. Introduction

This application note is a guide for migrating to the Macronix MX30LF4G18AC from the Spansion® S34ML04G200 4Gb, 3V, NAND flash memory.

The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 10. Newer versions of the datasheets may override the contents of this document.

## 2. Features

Both flash device families have similar features and functions as shown in Table 2-1.

**Table 2-1: Feature Comparison**

| Feature | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Vcc Voltage Range | 2.7V ~ 3.6V | 2.7V ~ 3.6V |
| Bus Width | x8 | x8 |
| Operating Temperature | -40℃ ~ 85℃ | -40℃ ~ 85℃ |
| Interface | ONFI 1.0 Standard | ONFI 1.0 Standard |
| Block Size | 128KB+**4KB** | 128KB+8KB |
| Page Size | 2KB+**64B** | 2KB+128B |
| ECC Requirement | 4b/528B | 4b/528B |
| OTP Size | 30 pages | 64 pages |
| Guarantee Good Blocks at Shipping | Block 0 | Block 0 & 1 |
| Unique ID | ONFI standard | ONFI standard |
| ID Code | **C2h**/DCh/90h/95h/56h | 01h/DCh/90h/95h/56h |
| ONFI Signature | 4Fh/4Eh/46h/49h | 4Fh/4Eh/46h/49h |
| Data Retention | 10 Years | 10 Years |
| Package | 48-TSOP (12x20mm)<br>63-VFBGA (9x11mm) | 48-TSOP (12x20mm)<br>63-VFBGA (9x11mm) |

# 3.Performance

Table 3-1 and Table 3-2 show MX30LF4G18AC and S34ML04G200 Read/Write performance.

**Table 3-1: Read Performance (Read Latency and Sequential Read)**

| Read function | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Read Latency time (tR) | 25us (max.) | 30us (max.) |
| Sequential Read time (tRC) | 20ns (min.) | 25ns (min.) |

**Table 3-2: Write Performance (Program and Erase)**

| Write Function | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Page Program time (tPROG) | 300us (typ.) / 600us (max.) | 300us (typ.) / 700us (max.) |
| Block Erase time (tERASE) | 1ms (typ.) / 3.5ms (max.) | 3.5ms (typ.) / 10ms (max.) |
| NOP | 4 (max.) | 4 (max.) |
| Write/Erase Cycles*[1] (Endurance) | 100,000 | 100,000 |

*Note: 100K Endurance cycle with ECC protection.*

# 4.DC Characteristics

Read/Write power requirements (Table 4-1) and I/O voltage limits (Table 4-2) are similar.

**Table 4-1: Read / Write Current**

| DC Characteristic | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Sequential Read Current (ICC1) | 20mA (typ.) / 30mA (max.) | 15mA (typ.) / 30mA (max.) |
| Program Current (ICC2) | 20mA (typ.) / 30mA (max.) | 15mA (typ.) / 30mA (max.) |
| Erase Current (ICC3) | 15mA (typ.) / 30mA (max.) | 15mA (typ.) / 30mA (max.) |
| Standby Current – CMOS | 10uA (typ.) / 50uA (max.) | 10uA (typ.) / 50uA (max.) |

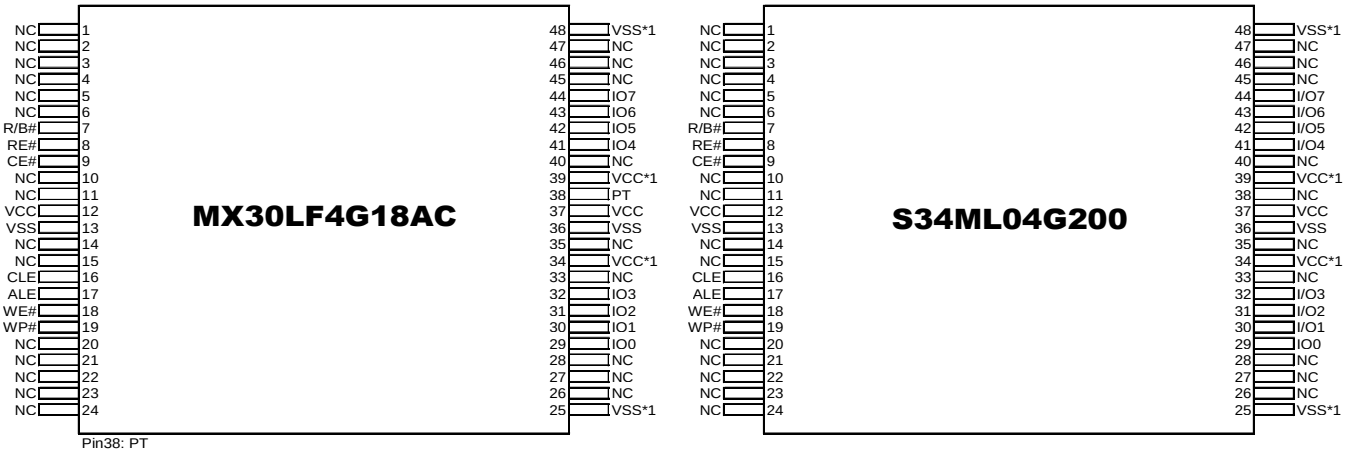
**Table 4-2: Input / Output Voltage**

| DC Characteristic | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Input Low Voltage (VIL) | -0.3V (min.) / 0.2VCC (max.) | -0.3V (min.) / 0.2Vcc (max.) |
| Input High Voltage (VIH) | 0.8VCC (min.) / VCC+0.3V (max.) | 0.8VCC (min.) / VCC+0.3V (max.) |
| Output Low Voltage (VOL) | 0.2V (max.) | 0.4V (max.) |
| Output High Voltage (VOH) | VCC-0.2V (min.) | 2.4V (min.) |

# 5. Package Pin/Ball Definition

Package physical dimensions are similar to each other. For detailed information, please refer to the individual datasheets. Tables 5-1 and 5-2 show differences in pin assignments between the Macronix and Spansion devices. The S34ML04G200 can be compared by the MX30LF4G18CA without pin conflicts. Only 48-TSOP pin #38 (63-VFBGA ball G5) may need special attention because the pin is designated “PT” which, if high during power-up, enables a memory protection function on the MX30LF4G18AC. The PT pin can be left unconnected as it has a weak internal pull-down to disable the protection feature.

**Figure 5-1: 48-TSOP (12x20mm) Package and Pin Layout Comparison**




Pin38: PT

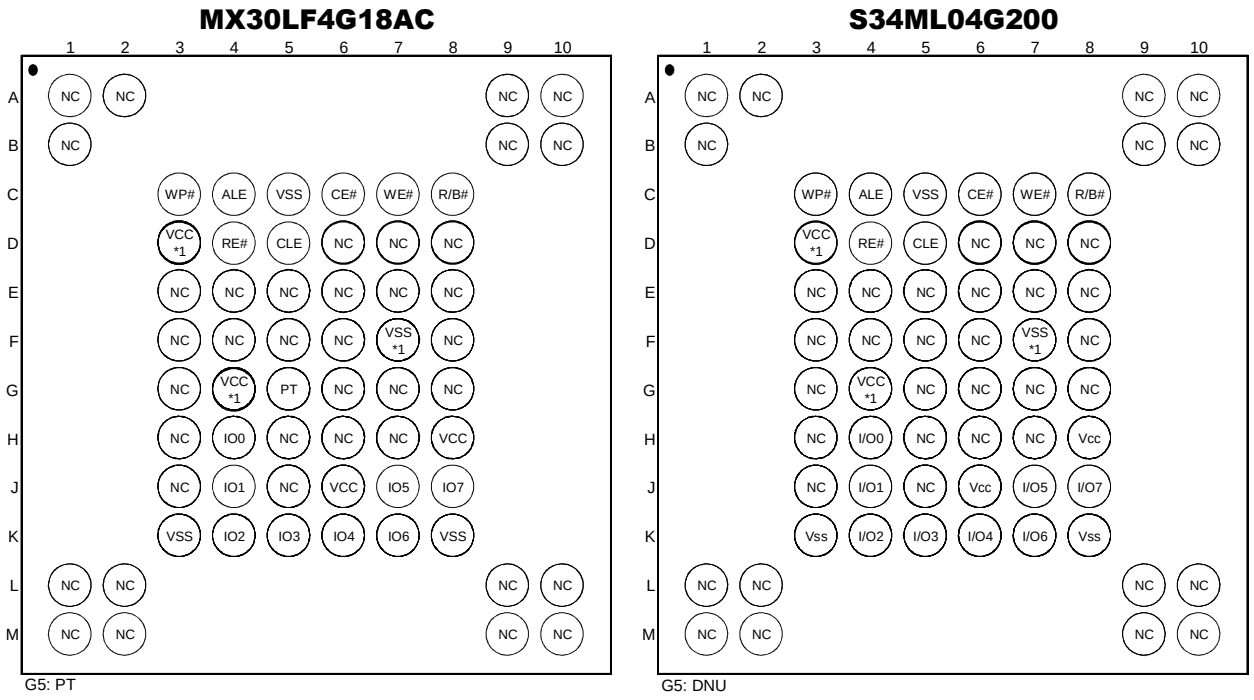
Note:
1. These pins might not be connected internally. However it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.

**Table 5-1: 48-TSOP Package Pin Definition**

| Brand | Macronix | Spansion |
|---|---|---|
| Part Name | MX30LF4G18AC-TI | S34ML04G200TFI00 |
| #38 pin | PT | NC |

*Note: The PT pin can be left unconnected as it has a weak internal pull-down to disable the protection feature. Please refer to the datasheet for more details.*

**Figure 5-2: 63-VFBGA (9x11mm) Package and Pin Layout Comparison**




Note:
1. These pins might not be connected internally. However it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.

**Table 5-2: 63-VFBGA Package Ball Definition**

| Brand | Macronix | Spansion |
|---|---|---|
| **Part Name** | **MX30LF4G18AC-XKI** | **S34ML04G200BHI00** |
| #G5 ball | PT | NC |

*Note: The PT pin can be left unconnected as it has a weak internal pull-down to disable the protection feature. Please refer to the datasheet for more details.*

## 6. Command Set

Basic command sets and status checking methods are similar. Read, Write, and Erase operation commands are identical (Table 6-1). Macronix implements the ONFI 2-Plane Block Erase command sequence (Table 6-2).

**Table 6-1: Command Table**

| Command | Macronix MX30LF4G18AC | | Spansion S34ML04G200 | |
|---|---|---|---|---|
| | 1st Cycle | 2nd Cycle | 1st Cycle | 2nd Cycle |
| Random Data Input | 85h | - | 85h | - |
| Random Data Output | 05h | E0h | 05h | E0h |
| Cache Read Begin | 00h | 31h | 31h | - |
| Read Mode | 00h | 30h | 00h | 30h |
| Cache Read End | 3Fh | - | 3Fh | - |
| Read ID | 90h | - | 90h | - |
| Reset | FFh | - | FFh | - |
| Page Program | 80h | 10h | 80h | 10h |
| Cache Program | 80h | 15h | 80h | 15h |
| Block Erase | 60h | D0h | 60h | D0h |
| Read Status | 70h | - | 70h | - |
| Read Parameter Pg. | ECh | - | ECh | - |
| Unique ID Read | EDh | | EDh | |
| Set Feature | EFh | | - | |
| Get Feature | EEh | | - | |
| Status Enhance Read | 78h | | 78h | |

**Table 6-2: Two-Plane Command Table**

| Command | Macronix MX30LF4G18AC | | | | Spansion S34ML04G200 | | | |
|---|---|---|---|---|---|---|---|---|
| | 1st Cycle | 2nd Cycle | 3rd Cycle | 4th Cycle | 1st Cycle | 2nd Cycle | 3rd Cycle | 4th Cycle |
| 2 Plane Program | - | - | - | - | 80h | 11h | 81h | 10h |
| ONFI 2 Plane Program | 80h | 11h | 80h | 10h | 80h | 11h | 80h | 10h |
| 2 Plane Cache Program | - | - | - | - | 80h | 11h | 81h | 15h |
| ONFI 2 Plane Cache Program | 80h | 11h | 80h | 15h | 80h | 11h | 80h | 15h |
| 2 Plane Block Erase | - | - | - | - | 60h | 60h | D0h | - |
| ONFI 2 Plane Block Erase | 60h | D1h | 60h | D0h | 60h | D1h | 60h | D0h |

### 6-2 Status Register

When a flash Read/Program/Erase operation is in progress, either the “Ready/Busy# Pin Checking” or “Status Output Checking” method may be used to monitor the operation. Both are standard NAND flash algorithms and can be used for both device families. Table 6-3 shows that Status Output content provided by the Read Status command (70h) is compatible. Table 6-4 shows that Two–plane Operation Status output provided by the Enhance Read command (78h) is compatible.

**Table 6-3: Status Output**

| Status Output | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| SR[0] | PGM/ERS status: Pass/Fail | PGM/ERS status: Pass/Fail |
| SR[1] | Cache Program status: Pass/Fail | Cache Program status: Pass/Fail |
| SR[2] | Reserved | Reserved |
| SR[3] | Reserved | Reserved |
| SR[4] | Reserved | Reserved |
| SR[5] | PGM/ERS/Read internal controller: Ready/Busy | PGM/ERS/Read internal controller: Ready/Busy |
| SR[6] | PGM/ERS/Read status: Ready/Busy | PGM/ERS/Read status: Ready/Busy |
| SR[7] | Write Protect | Write Protect |

**Table 6-4: Two-plane Status Output**

| Status Output | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| SR[0] | Selected Plane PGM/ERS status: Pass/Fail | Selected Plane PGM/ERS status: Pass/Fail |
| SR[1] | Selected Plane Cache Program status: Pass/Fail | Selected Plane Cache Program status: Pass/Fail |
| SR[2] | Reserved | Reserved |
| SR[3] | Reserved | Reserved |
| SR[4] | Reserved | Reserved |
| SR[5] | PGM/ERS/Read internal controller: Ready/Busy | PGM/ERS/Read internal controller: Ready/Busy |
| SR[6] | PGM/ERS/Read status: Ready/Busy | PGM/ERS/Read status: Ready/Busy |
| SR[7] | Write Protect | Write Protect |

# 7. Read ID Command

The ID of the Macronix MX30LF4G18AC begins with a one-byte Manufacturer Code followed by a four-byte Device ID. While the same command set is used to read the Manufacturer ID, Device ID, and flash structure, the IDs are different, allowing software to identify the device manufacturer and device type (Table 7-1).

**Table 7-1: Manufacturer and Device IDs**

| ID code | | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|---|
| Value | | **C2h**/DCh/90h/95h/56h | **01h**/DCh/90h/95h/56h |
| 1st Byte | | Manufacturer Code | Manufacturer Code |
| 2nd Byte | | Device Identifier | Device Identifier |
| 3rd Byte | IO1, IO0 | Number of Die per Chip Enable | Number of Die per Chip Enable |
| | IO3, IO2 | Cell Structure | Cell Structure |
| | IO5, IO4 | Number of Simultaneously Programmed Pages | Number of Simultaneously Programmed Pages |
| | IO6 | Interleaved Programming Between Multiple Chips | Interleaved Programming Between Multiple Chips |
| | IO7 | Cache Programming | Cache Programming |
| 4th Byte | IO1, IO0 | Page Size (exclude Spare Area) | Page Size (exclude Spare Area) |
| | IO2 | Size of Spare Area (Byte per 512Byte) | Size of Spare Area (Byte per 512Byte) |
| | IO7, IO3 | Sequential Read Cycle Time (tRC) | Serial Access Time (tRC) |
| | IO5, IO4 | Block Size (exclude Spare Area) | Block Size (exclude Spare Area) |
| | IO6 | Organization | Organization |
| 5th Byte | IO0, IO1 | **ECC Level Requirement** | Reserved |
| | IO2, IO3 | Number of Planes per CE | Number of Planes per CE |
| | IO4~IO6 | Plane Size | Plane Size |
| | IO7 | Reserved | Reserved |

## 8. Power-Up Timing

Macronix and Spansion® power-up sequences are similar, but the timing is slightly different. Although both devices use 2.7V (VCC min.) as the start point, timing references are different. Check the system timing to determine if adjustments are needed.

**Table 8-1: Power-Up Timing**

| H/W Timing Characteristic | Macronix MX30LF4G18AC | Spansion S34ML04G200 |
|---|---|---|
| Vcc (min.) to WE# low | 1ms (max.) | N/A |
| Vcc (min.) to R/B# high | N/A | 5ms (max.) |
| Vcc (min.) to R/B# low | 10us (max.) | 100us (max.) |

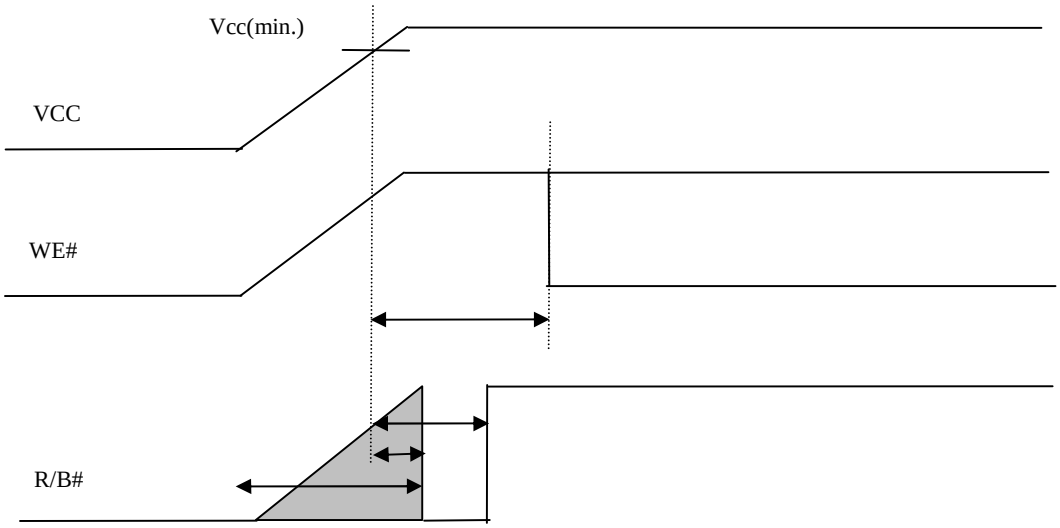



**Figure 8-1: Power-Up Timing**

## 9. Summary

Macronix MX30LF4G18AC and Spansion® S34ML04G200 NAND have similar features and pin outs. Because basic Read/Program/Erase commands are the same, device migration may require minimal firmware modifications primarily due to differences in spare area sizes.

# 10. Reference

Table 10-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix website at http://www.macronix.com

**Table 10-1: Datasheet Version**

| Datasheet | Location | Date Issue | Revision |
|---|---|---|---|
| MX30LF4G18AC | - | Sept. 5, 2014 | Rev. 0.02 |
| S34ML04G200 | Website | Sept. 5, 2014 | Rev. 10 |

*Note: Macronix data sheet is subject to change without notice.*

# 11. Appendix

Cross Reference Table 11-1 shows basic part number and package information for the Macronix MX30LF4G18AC and Spansion® S34ML04G200 product.

**Table 11-1: Part Number Cross Reference**

| Density | Macronix Part No. | Spansion Part No. | Package | Dimension |
|---|---|---|---|---|
| 4Gb | MX30LF4G18AC-TI | S34ML04G200TFI00 | 48-TSOP | 12x20mm |
| 4Gb | MX30LF4G18AC-XKI | S34ML04G200BHI00 | 63-VFBGA | 9x11mm |

# 12. Revision History

| Revision | Description | Date |
|---|---|---|
| 1.0 | Initial Release | Oct.13 , 2014 |

# Comparing Spansion® S34ML04G200 with Macronix MX30LF4G18AC

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