MACRONIX
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APPLICATION NOTE

Migrating to MX25L1606E / MX25L8006E from MX25L1605D / MX25L8005

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Contents

Migrating to MX25L1606E / MX25L8006E from MX25L1605D / MX25L8005

1. Introduction

This application note indicates the differences between MX25L1606E/MX25L8006E and MX25L1605D /MX25L8005.

In Single I/O mode, MX25L1606E and MX25L8006E are identical in forms and functions with MX25L1605D and MX25L8005. MX25L1606E and MX25L8006E are capable of Dual Output mode (Single Input / Dual Output) but no longer support x2 I/O (Dual Input / Dual Output) mode and Continuous Program (CP) mode. The comparison and features of new products are described in the following sections.

The information provided is based on the data available at the time. The MX25L1606E and MX25L8006E datasheet may override this application note if there is a difference description for the same in the datasheet.

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2. General Features

2-1. Feature Comparison

The Dual Output mode (1I/2O) is one of the new features of MX25L1606E and MX25L8006E, and this new product accepts wide range of clock rate from DC (Direct Current)~ 86MHz.

Table 2-1: Major Feature Comparison of 8Mb Devices

Feature	MX25L8005	MX25L8006E
Voltage	2.7 to 3.6V	2.7 to 3.6V
Interface	x1	x1, 1I/2O*
Package	8-SOP(150mil/209mil) 8-WSON(6x5mm) 8-USON(4x4mm) 8-PDIP(300mil)	8-SOP(150mil/209mil) 8-WSON(6x5mm) 8-USON(4x4mm) 8-PDIP(300mil)
Operation Temperature	-40°C to 85°C	-40°C to 85°C
Sector Structure	4KB	4KB
Block Structure	64KB	64KB
Clock Rate	86MHz	86MHz
Byte Program	No	**Yes**
CP (Continuous Program) Mode	No	No
OTP	No	**512 bits**
Security Register	No	**Yes**
Endurance (typ.)	100k	100k
Data Retention	20y	20y

***Note:** MX25L8006E in Dual Output mode is single input, dual output (1I/2O).*

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Table 2-2: Major Feature Comparison of 16Mb Devices

Feature	MX25L1605D	MX25L1606E
Voltage	2.7 to 3.6V	2.7 to 3.6V
Interface	x1, x2	x1, 1I/2O*
Package	8-SOP (150mil/209mil) 8-WSON (6x5mm) 8-USON (4x4mm) 8-PDIP (300mil)	8-SOP (150mil/209mil) 8-WSON (6x5mm) 8-USON (4x4mm) 8-PDIP (300mil)
Operation Temperature	-40°C to 85 °C	-40°C to 85 °C
Sector Structure	4KB	4KB
Block Structure	64KB	64KB
Clock Rate	86MHz	86MHz
Byte Program	Yes	Yes
CP (Continuous Program) Mode	Yes	**No**
OTP	512 bits	**512 bits**
Security Register	Yes	Yes
Endurance (typ.)	100k	100k
Data Retention	20y	20y

***Note:** MX25L1606E in Dual Output mode is single input, dual output (1I/2O).*

2-2. Command Set Comparison

The new product adds new command Double Output Mode Command (DREAD) for the new feature.

Table 2-3: Command Table Comparison of 8Mb Devices

Command	MX25L8005	MX25L8006E
WREN (Write Enable)	06	06
WRDI (Write Disable)	04	04
RDID (Read Identification)	9F	9F
RDSR (Read Status Register)	05	05
WRSR (Write Status Register)	01	01
READ (Read Data)	03	03
FATS READ (Fast Read Data)	0B	0B
DREAD (Dual Output Read Command)	--	**3B**
SE (Sector Erase)	20	20
BE (Block Erase)	52 or D8	52 or D8
CE (Chip Erase)	60 or C7	60 or C7
PP (Page Program)	02	02
DP (Deep Power Down)	B9	B9
RDP (Release from Deep Power Down)	AB	AB
RES (Read Electronic ID)	AB	AB
REMS (Read Electronic Manufacturer & Device ID)	90	90
ENSO (Enter Secured OTP)	--	**B1**
EXSO (Exit Secured OTP)	--	**C1**
RDSCUR (Read Security Register)	--	**2B**
WRSCUR (Write Security Register)	--	**2F**

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Table 2-4: Command Table Comparison of 16Mb Devices

Command	MX25L1605D	MX25L1606E
WREN (Write Enable)	06	06
WRDI (Write Disable)	04	04
RDID (Read Identification)	9F	9F
RDSR (Read Status Register)	05	05
WRSR (Write Status Register)	01	01
READ (Read Data)	03	03
FATS READ (Fast Read Data)	0B	0B
2READ (Dual I/O Read Command)	**BB**	--
DREAD (Dual Output Read Command)	--	**3B**
SE (Sector Erase)	20	20
BE (Block Erase)	**D8**	**52 or D8**
CE (Chip Erase)	60 or C7	60 or C7
PP (Page Program)	02	02
CP (Continuous Program Mode)	**AD**	--
DP (Deep Power Down)	B9	B9
RDP (Release from Deep Power Down)	AB	AB
RES (Read Electronic ID)	AB	AB
REMS (Read Electronic Manufacturer & Device ID)	90	90
REMS2 (Read ID for Dual I/O Mode)	**EF**	--
ENSO (Enter Secured OTP)	B1	B1
EXSO (Exit Secured OTP)	C1	C1
RDSCUR (Read Security Register)	2B	2B
WRSCUR (Write Security Register)	2F	2F
ESRY (Enable SO to Output RY/BY#)	**70**	--
DSRY (Disable SO to Output RY/BY#)	**80**	--

2-3. AC and DC Specifications Comparison

Table 2-5: AC & DC Characteristic Comparison of 8Mb Devices

Characteristic	MX25L8005	MX25L8006E
ISB1	10uA	25uA
ICC2	15mA	20mA
ICC5	15mA	20mA
tSHSL	100 ns	15ns (read), 40ns (write)

Table 2-6: AC & DC Characteristic Comparison of 16Mb Devices

Characteristic	MX25L1605D	MX25L1606E
ISB1	20uA	25uA
fTSCLK	10k to 50MHz	DC to 80MHz
tCLQV	10/8 ns	8/6 ns
tHHQX	10 ns	6ns
tHLQZ	10ns	6ns
tSHSL	40ns	15ns (read), 40ns (write)

3. Device ID

Table 3-1: Device ID Comparison of 8Mb Devices

Command Type	MX25L8005	MX25L8006E	Remarks
Manufacturer ID	C2	C2	
Electric ID	13	13	RES Command
REMS	C2,20,14	C2,20,14	RDID Command

Table 3-2: Device ID Comparison of 16Mb Devices

Command Type	MX25L1605D	MX25L1606E	Remarks
Manufacturer ID	C2	C2	
Electric ID	14	14	RES Command
REMS	C2,20,15	C2,20,15	RDID Command

4. References

The following datasheets were used for preparing this comparison note:

Datasheet	Location	Date Issued	Versions
MX25L8005	Macronix Website	June 05, 2009	2.3
MX25L8006E	Macronix Website	October 16, 2014	1.5
MX25L1605D	Macronix Website	April 29, 2009	1.5
MX25L1606E	Macronix Website	June 04, 2015	1.8

For more functional and parametric specifications, please refer to the datasheet on the Macronix Website at http://www.macronix.com/ and go to: Products/Serial NOR Flash.

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Revision History

Revision No.	Description	Page	Date
1.1	1. Modified Table 2-1, 2-2 and 2-3	P2-3	FEB/04/2010
1.2	1. Modified DMC description	P6	MAR/31/2010
	2. Revised notes for 1I/2O	P2-3	
	3. Revised Table 2-1	P2	
	4. Changed DMC wording to SFDP	All	JUN/01/2010
	5. Revised Introduction	P2	
	6. Revised Table 3-1. 3-2	P8	
	7. Removed SFDP	All	JUL/2/2010
4	1. Removed ACC Mode descriptions	P3-4	JAN/18/2017
	2. Changed ISB1 from 50uA to 25uA	P7	
	3. Changed tSHSL (write) from 50ns to 40ns	P7	
	4. Modified fT/(Min.) from 10KHz to DC	P7	
	5. Updated *"4. References"*	P8	
	6. Updated the numbering format to align with the new internal rule	All	

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