

Comparing Toshiba® TC58BVG0S3H with Macronix MX30LF1GE8AB

1. Introduction

This application note is a guide for migrating to the Macronix MX30LF1GE8AB from the Toshiba TC58BVG0S3H 1Gb, 3V, Internal ECC NAND flash memory.

The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information in this document is based on datasheets listed in Section 11. Newer versions of the datasheets may override the contents of this document.

2. Features

Both flash device families have similar features and functions as shown in Table 2-1.

Table 2-1: Feature Comparison

Feature	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Vcc Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Bus Width	x8	x8
Operating Temperature	-40°C ~ 85°C	-40°C ~ 85°C
Interface	ONFI 1.0 Compliant	-
Block Size	128KB+4KB	128KB+4KB
Page Size	2KB+64B	2KB+64B
Internal ECC Capability	4b/540B	8b/528B
OTP Size	30 pages	-
Guaranteed Good Blocks at Shipping	Block 0	Block 0
Unique ID	ONFI Compliant	-
First Command	-	Reset (FFh)
ID Code	C2h/F1h/80h/95h/82h	98h/F1h/80h/15h/F2h
ONFI Signature	4Fh/4Eh/46h/49h	-
Data Retention	10 Years	-
Package	48-TSOP (12x20mm) 63-VFBGA (9x11mm) 48-VFBGA (6x8mm)	48-TSOP (12x20mm) 63-VFBGA (9x11mm) 67-VFBGA (6.5x8mm)

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3. Performance

Table 3-1 and Table 3-2 show MX30LF1GE8AB and TC58BVG0S3H Read/Write performance.

Table 3-1: Read Performance (Read Latency and Sequential Read)

Read function	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Read Latency time (tR_ECC)	45us (typ.) / 70us (max.)	40us (typ.) / 120us (max.)
Sequential Read time (tRC)	20ns (min.)	25ns (min.)

Table 3-2: Write Performance (Program and Erase)

Write Function	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Page Program time (tPROG_ECC)	320us (typ.) / 600us (max.)	330us (typ.) / 700us (max.)
Block Erase time (tERASE)	1ms (typ.) / 3.5ms (max.)	2.5ms (typ.) / 5ms (max.)
NOP	4 (max.)	4 (max.)
Write/Erase Cycles* ¹ (Endurance)	100,000	-

Note: 100K Endurance cycle with ECC protection.

4. DC Characteristics

Read/Write power requirements (Table 4-1) and I/O voltage limits (Table 4-2) are similar.

Table 4-1: Read / Write Current

DC Characteristic	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Sequential Read Current (ICC1)	20mA (typ.) / 30mA (max.)	30mA (max.)
Program Current (ICC2)	20mA (typ.) / 30mA (max.)	30mA (max.)
Erase Current (ICC3)	15mA (typ.) / 30mA (max.)	30mA (max.)
Standby Current – CMOS	10uA (typ.) / 50uA (max.)	50uA (max.)

Table 4-2: Input / Output Voltage

DC Characteristic	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Input Low Voltage (VIL)	-0.3V (min.) / 0.2VCC (max.)	-0.3V (min.) / 0.2VCC (max.)
Input High Voltage (VIH)	0.8VCC (min.) / VCC+0.3V (max.)	0.8VCC (min.) / VCC+0.3V (max.)
Output Low Voltage (VOL)	0.2V (max.)	0.2V (max.)
Output High Voltage (VOH)	VCC-0.2 (min.)	VCC-0.2 (min.)

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5. Package Pin Definition

Package physical dimensions are similar to each other. For detailed information, please refer to the individual datasheets. Table 5-1, Table 5-2, and Table 5-3 show the differences in pin assignments between the Macronix and Toshiba devices. The TC58BVG0S3H can be compared to the MX30LF1GE8AB. 48-TSOP pin #38 or 63-VFBGA ball G5 may need special attention because the pin is designated as DNU on the MX30LF1GE8AB, but TC58BVG0S3H is designated as NC. The TC58BVG0S3H offers a 67-VFBGA package, but the MX30LF1GE8AB offers a 48-VFBGA package. Both packages can be compared by by using the middle 48 ball locations only. 48-VFBGA ball E3 and 67-VFBGA ball F4 may need special attention because the pin is designated as DNU on the MX30LF1GE8AB, but on the TC58BVG0S3H it is designated as NC.

Figure 5-1: 48-TSOP (12x20mm) Package and Pin Layout Comparison

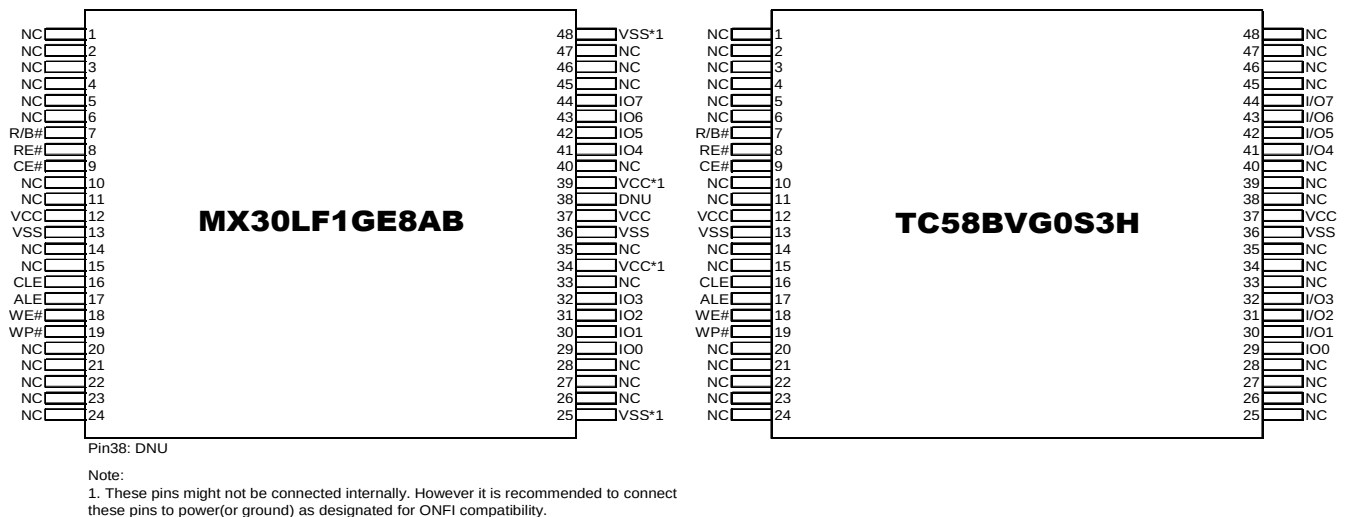


Table 5-1: 48-TSOP Package Pin Different Definition Comparison

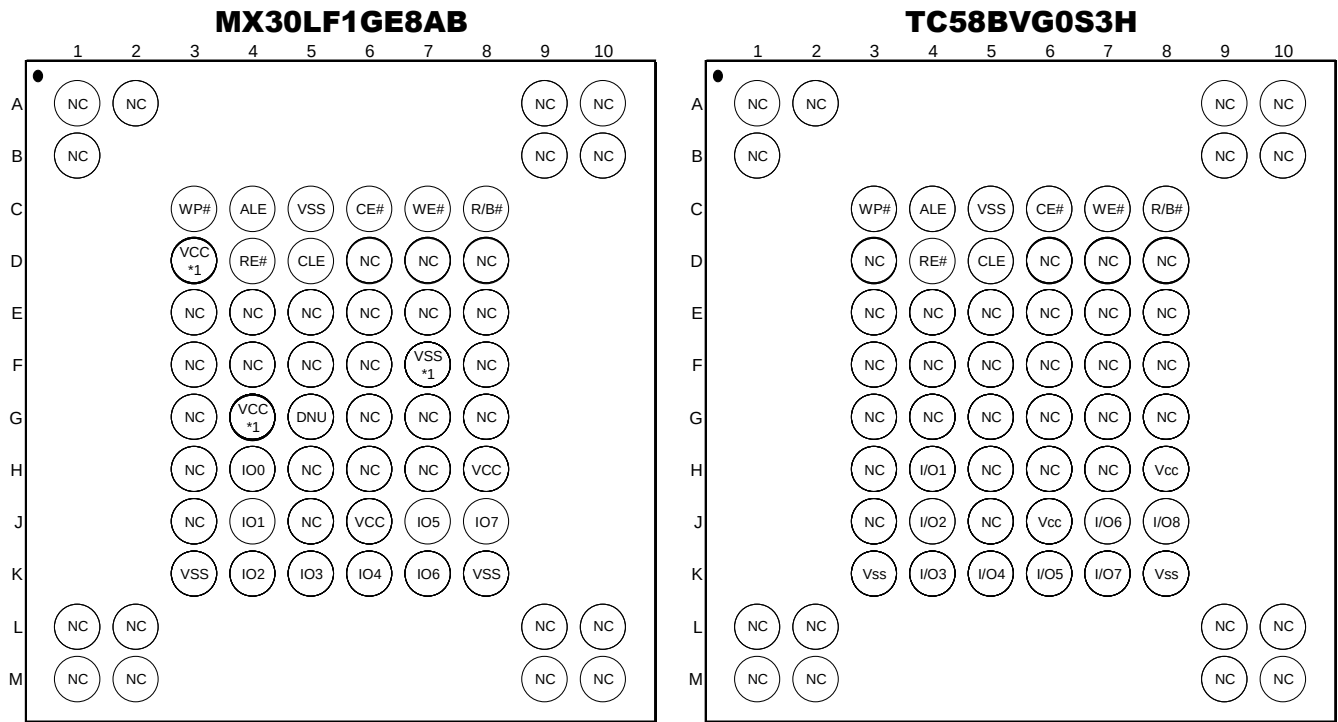
Pin	Macronix MX30LF2G28AC-TI	Toshiba TC58NVG1S3HTAI0
48	VSS ⁽²⁾ , Recommend to Connect to VSS	NC
39	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
38	DNU ⁽¹⁾	NC ⁽¹⁾
34	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
25	VSS ⁽²⁾ , Recommend to Connect to VSS	NC

Note: 1. DNU = Do not use; NC = No Connect

2. This pin is ONFI Compliant which is designated for ONFI compatibility.

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Figure 5-2: 63-VFBGA (9x11mm) Package and Pin Layout Comparison



G5: DNU

Note:

1. These pins might not be connected internally. However it is recommended to connect these pins to power(or ground) as designated for ONFI compatibility.

Table 5-2: 63-VFBGA Package Ball Different Definition Comparison

Ball	Macronix MX30LF1GE8AB-XKI	Toshiba TC58BVG0S3HBAI4
D3	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
F7	VSS ⁽²⁾ , Recommend to Connect to VSS	NC
G4	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
G5	DNU ⁽¹⁾	NC

Note: 1. DNU = Do not use; NC = No Connect

2. This pin is ONFI Compliant which is designated for ONFI compatibility.

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Figure 5-3: 48-VFBGA (6x8mm)/67-VFBGA (6.5x8mm) Package and Pin Layout Comparison

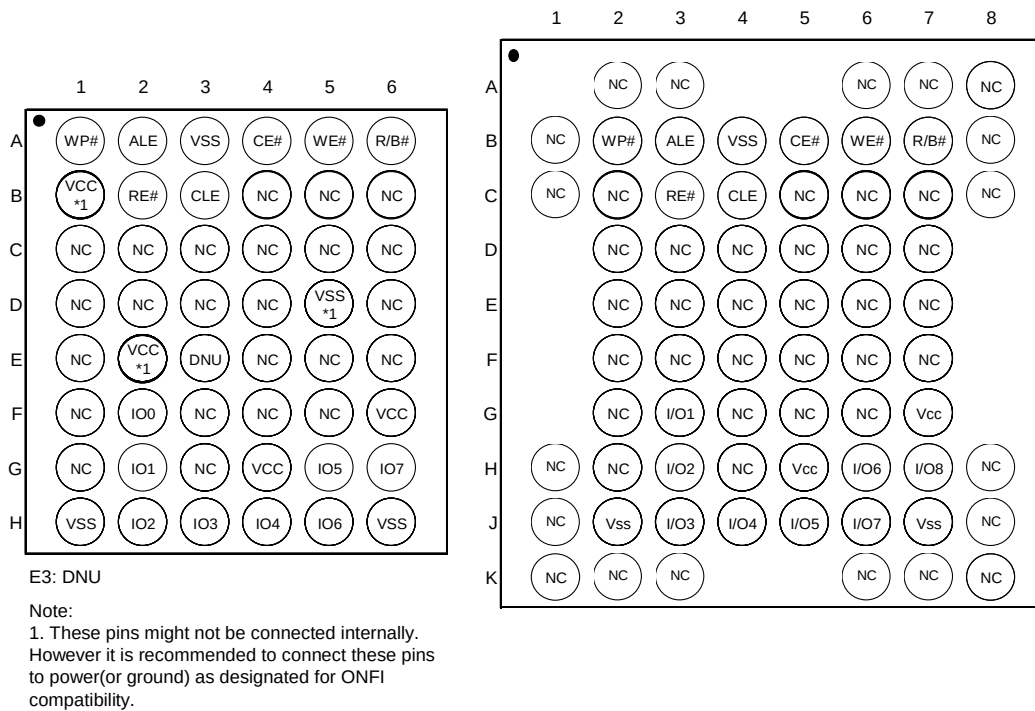


Table 5-3: 48-VFBGA/67-VFBGA Package Ball Different Definition Comparison

Ball(48-VFBGA/67-VFBGA)	Macronix MX30LF1GE8AB-XQI	Toshiba TC58BVG0S3HBAI6
B1/C2	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
D5/E6	VSS ⁽²⁾ , Recommend to Connect to VSS	NC
E2/F3	VCC ⁽²⁾ , Recommend to Connect to VCC	NC
E3/F4	DNU ⁽¹⁾	NC
-/A2,A3, A6,A7,A8 -/B1,B8,C1,C8 -/H1,H8,J1,J8 -/K1,K2,K3,K6,K7,K8	N/A ⁽³⁾	NC

Note: 1. DNU = Do not use; NC = No Connect

2. This pin is ONFI Compliant which is designated for ONFI compatibility.

3. Middle 48 balls of 67-VFBGA are same ball size, ball pitch as 48-VFBGA package. Different ball function refers to Table 5-3. The outside surrounding balls are NC in 67-VFBGA package. User could follow a layout rule providing for a dual layout for 48-VFBGA and 67-VFBGA package. This application note will not discuss detail information about dual layout schemes.

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6. Command Set

6-1 Basic Commands

Basic command sets and status checking methods are similar. The Read and Write operation commands are similar. (Table 6-1).

Table 6-1: Command Table

Command	Macronix MX30LF1GE8AB		Toshiba TC58BVG0S3H	
	1st Cycle	2nd Cycle	1st Cycle	2nd Cycle
Serial Data Input	-	-	80h	-
Page Read	00h	30h	00h	30h
Random Data Input	85h	-	85h	-
Random Data Output	05h	E0h	05h	E0h
Read ID	90h	-	90h	-
Reset	FFh	-	FFh	-
Page Program	80h	10h	80h	10h
Cache Program	80h	15h	-	-
Block Erase	60h	D0h	60h	D0h
Read Status	70h	-	70h	-
ECC Status Read	-	-	7Ah	
Parameter Page Read	ECh	-	-	-
Unique ID Read	EDh	-	-	-
Set Feature	EFh	-	-	-
Get Feature	EEh	-	-	-

6-2 Status Register

When a Read, Program, or Erase operation is in progress, either the “Ready/Busy# Pin Checking” or “Status Output Checking” method may be used to monitor the operation. Both are standard NAND flash algorithms and can be used for both device families. Table 6-3 compares the Status Output provided by the Read Status command (70h).

Macronix and Toshiba report ECC correction status in the Status Register, but bit usage and definitions are slightly different. Macronix uses SR[3] and SR[4] in combination with SR[0] to show detailed ECC correction status, so that user can decide when to rewrite data. Table 6-4 shows the meaning of each combination result.

Toshiba provides an ECC Status Read function (7Ah command) to check ECC correction status. ECC Status Register, SR[0]~SR[3] indicate the correction status, and SR[4]~SR[7] indicate the sector information. Table 6-5 and Table 6-6 show the meaning of each combination result.

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Table 6-3: Status Output

Status Bit	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
SR[0]	Chip PGM/ERS/READ status: Pass/Fail	Chip PGM/ERS/READ status: Pass/Fail
SR[1]	Cache Program status: Pass/Fail	Reserved
SR[2]	Reserved	Reserved
SR[3]	Internal ECC Status* ¹	Rewrite Recommended
SR[4]	Internal ECC Status* ¹	Reserved
SR[5]	PGM/ERS/Read internal controller: Ready/Busy	PGM/ERS/Read status: Ready/Busy
SR[6]	PGM/ERS/Read status: Ready/Busy	PGM/ERS/Read status: Ready/Busy
SR[7]	Write Protect	Write Protect

Note: For Macronix internal ECC status, refer to Table 6-4.

Table 6-4: Macronix Internal ECC Bits Status

SR bits and value			Status of ECC correction
SR[4]	SR[3]	SR[0]	
0	0	1	Uncorrectable
0	0	0	0 or 1-bit error corrected
1	0	0	2-bit error corrected
0	1	0	3-bit error corrected
1	1	0	4-bit error corrected

Table 6-5: Toshiba Internal ECC Bits Status

ECC_SR bits and value				Status of ECC correction
SR[3]	SR[2]	SR[1]	SR[0]	
0	0	0	0	No Error
0	0	0	1	1-bit error and correctable
0	0	1	0	2-bit error and correctable
0	0	1	1	3-bit error and correctable
0	1	0	0	4-bit error and correctable
0	1	0	1	5-bit error and correctable
0	1	1	0	6-bit error and correctable
0	1	1	1	7-bit error and correctable
1	0	0	0	8-bit error and correctable
1	1	1	1	Uncorrectable

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Table 6-6: Toshiba Sector information Bits Status for ECC

ECC_SR bits and value				Sector Information
SR[7]	SR[6]	SR[5]	SR[4]	
0	0	0	0	1 st Sector (Main and Spare area)
0	0	0	1	2 nd Sector (Main and Spare area)
0	0	1	0	3 rd Sector (Main and Spare area)
0	0	1	1	4 th Sector (Main and Spare area)
Other				Reserved

7. Read ID Command

The ID of the Macronix MX30LF1GE8AB begins with a one-byte Manufacturer Code followed by a four-byte Device ID. While the same command set is used to read the Manufacturer ID, Device ID, and flash structure, the IDs are different, allowing software to identify the device manufacturer and device type (Table 7-1).

Table 7-1: Manufacturer and Device IDs

ID code		Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Value		C2h/F1h/80h/95h/82h	98h/F1h/80h/15h/F2h
1 st Byte		Manufacturer Code	Manufacturer Code
2 nd Byte		Device Identifier	Device Identifier
3 rd Byte	IO1, IO0	Number of Die per Chip Enable	Number of Die per Chip Enable
	IO3, IO2	Cell Structure	Cell Structure
	IO5, IO4	Number of Simultaneously Programmed Pages	Reserved
	IO6	Interleaved Programming Between Multiple Chips	Reserved
	IO7	Cache Program	Reserved
4 th Byte	IO1, IO0	Page Size (excluding Spare Area)	Page Size (excluding Spare Area)
	IO2	Spare Area Size	Reserved
	IO7, IO3	Sequential Read Cycle Time (tRC)	Reserved
	IO5, IO4	Block Size (excluding Spare Area)	Block Size (exclude Spare Area)
	IO6	Organization	Organization
5 th Byte	IO1, IO0	ECC Level Requirement	Reserved
	IO3, IO2	Number of Planes per CE	Number of Planes per CE
	IO6~IO4	Plane Size	Reserved
	IO7	Internal ECC Enabled/Disabled	Internal ECC Enabled/Disabled

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8. Internal ECC Function

8-1 Enabling Internal ECC

Macronix and Toshiba provide Internal ECC functions which generate ECC code internally when programming data into the memory array. The Internal ECC function is always enabled in both devices.

8-2 Internal ECC Protected Areas

Macronix provides 4-bit ECC correction and Toshiba[®] provides 8-bit ECC correction. Table 8-1 shows the areas protected by the Internal ECC function. Each spare area is associated with its corresponding main array area. For example, Spare Area 0 is associated with Main Array 0 only. Both the Macronix and Toshiba[®] devices have a maximum NOP (Number of Partial-Page) programming limitation of 4, so the user needs to program the main array and corresponding spare area together during a single programming operation.

Table 8-1: Internal ECC Protection Area

Device	Main Array (2KB)				Spare Area (64B)			
	Main 0	Main 1	Main 2	Main 3	Spare 0	Spare 1	Spare 2	Spare 3
MX30LF1GE8AB	512B	512B	512B	512B	16B	16B	16B	16B
TC58BVG0S3H	512B	512B	512B	512B	16B	16B	16B	16B

together during a single programming operation.

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9. Power-Up Timing

Macronix and Toshiba power-up sequences are similar, but the timing is slightly different. Although both devices use 2.7V (VCC min.) as the start point, measurement items are different. Check the system timing to determine if adjustments are needed.

Table 9-1: Power-Up Timing

H/W Timing Characteristic	Macronix MX30LF1GE8AB	Toshiba TC58BVG0S3H
Vcc (min.) to WE# low	1ms (max.)* ¹	N/A
Vcc (min.) to R/B# high	N/A	1ms (max.)
Vcc (min.) to R/B# low	10us (max.)	100us (max.)

Note: Macronix requires an initialization delay during power on.

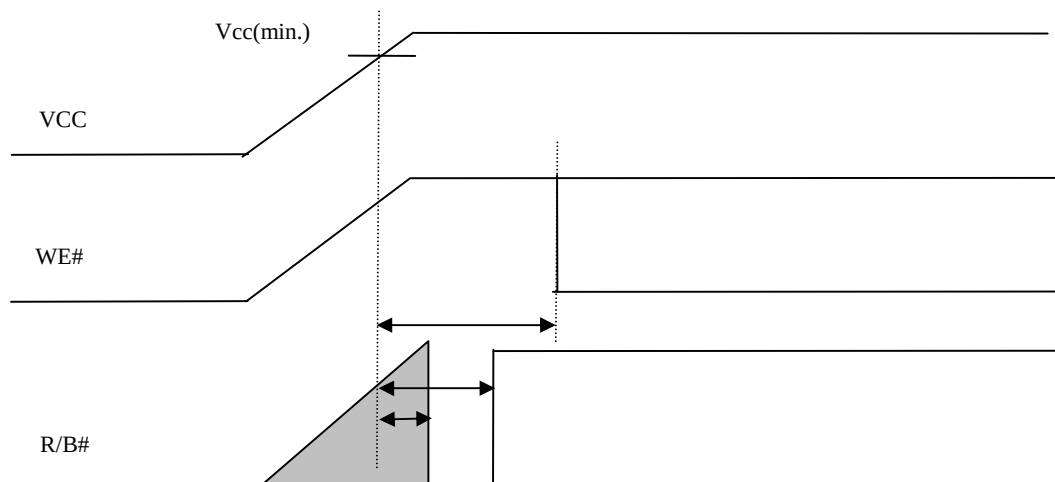


Figure 9-1: Power-Up Timing

10. Summary

The Macronix MX30LF1GE8AB and Toshiba TC58BVG0S3H NAND have similar features and pinouts. While basic Read, Program, and Erase commands are the same, more advanced features such as Internal ECC status bits differ slightly. Overall, device migration may require minimal software modifications.

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11. Reference

Table 11-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix website at <http://www.macronix.com>

Table 11-1: Datasheet Version

Datasheet	Location	Date Issue	Revision
MX30LF1GE8AB	Website	Nov. 17, 2015	Rev. 1.3
TC58BVG0S3HTAI0	Website	Aug. 31, 2012	Rev. 1.00
TC58BVG0S3HBAI4	Website	Oct. 01, 2012	Rev. 1.00
TC58BVG0S3HBAI6	Website	Aug. 31, 2012	Rev. 1.00

Note: Macronix data sheet is subject to change without notice.

12. Appendix

Cross Reference Table 12-1 shows basic part number and package information for the Macronix MX30LF1GE8AB and Toshiba TC58BVG0S3H.

Table 12-1: Part Number Cross Reference

Density	Macronix Part No.	Toshiba Part No.	Package	Dimension
1Gb	MX30LF1GE8AB-TI	TC58BVG0S3HTAI0	48-TSOP	12x20mm
1Gb	MX30LF1GE8AB-XKI	TC58BVG0S3HBAI4	63-VFBGA	9x11mm
1Gb	MX30LF1GE8AB-XQI	TC58BVG0S3HBAI6-	48-VFBGA	6x8mm

13. Revision History

Revision	Description	Date
1.0	Initial Release	Jan. 28 , 2015
2.0	Add 63-BGA & 48-BGA package information	Apr. 20, 2017



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APPLICATION NOTE

Comparing Toshiba[®] TC58BVG0S3H with Macronix MX30LF1GE8AB

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