Migrating from MX25U25635F to MX25U25645G

1. Introduction

This document highlights parameters which may require attention when migrating from the MX25U25635F (75nm “F” Version) to the MX25U25645G (55nm “G” Version).

Generally, the G version is backward compatible with the F version as it is pin and command compatible with the basic Read/Program/Erase commands. There may be some differences if special features are used such as “DTR mode” and “Advanced Sector Protection”.

The document does not provide detailed information on the individual devices, but highlights the major similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information provided in this document is based on datasheets listed in Section *"10. Reference Documents"*. Newer versions of the datasheets may override the contents of this document. A comparison of key features is provided in *"Table 1-1: Key Feature Comparison"*.

Table 1-1: Key Feature Comparison

Feature		Part Number	
		MX25U25635F	**MX25U25645G**
Process Technology		75nm	55nm
VCC		1.65V – 2V	1.65V – 2V
I/O		x1/x2/x4	x1/x2/x4
Sector Size	4KB	Yes	Yes
	32KB	Yes	Yes
	64KB	Yes	Yes
Program Buffer Size		256Byte	256Byte
Security OTP		4KBit	4KBit
Read Interface	Normal Read	50MHz	50MHz
	Fast Read 1x I/O	108MHz	133MHz
	Fast Read 2x I/O	84MHz (4 dummy cycles) 133MHz (10 dummy cycles)	84MHz (4 dummy cycles) 166MHz (10 dummy cycles)
	Fast Read 4x I/O	84MHz (6dummy cycles) 133MHz (10 dummy cycles)	84MHz (6 dummy cycles) 133MHz (10 dummy cycles)
DTR (4x I/O)		NA	100MHz (10 dummy cycles)
Features			
QPI Interface		Yes	Yes
Read Enhance Mode		Yes	Yes
Wrap around read mode		Yes	Yes
Configurable dummy cycle		Yes	Yes
Adjustable output driver		Yes	Yes
Suspend & Resume		Yes	Yes
Fast Boot (XIP) Mode		Yes	Yes
BP Protection		Yes	Yes
Password protection		NA	Yes
Volatile write protection		NA	Yes
Non-volatile Write Protection		NA	Yes
SFDP		JESD216	JESD216B

2. Package

MX25U25645G provides 16-SOP (300mil) and 8-WSON (8x6mm) package options, which have pin out and physical dimensions identical to the MX25U25635F.

For more package information, please refer to the datasheets or contact our regional sales.

Table 2-1: Package Pins Comparison

16-PIN SOP (300mil)				
MX25U25645G	**MX25U25635F**		**MX25U25635F**	**MX25U25645G**
NC/SIO3	DNU/SIO3	1 / 16	SCLK	SCLK
VCC	VCC	2 / 15	SI/SIO0	SI/SIO0
RESET#	RESET#	3 / 14	NC	NC
NC	NC	4 / 13	NC	NC
DNU	NC	5 / 12	NC	DNU
DNU	NC	6 / 11	NC	DNU
CS#	CS#	7 / 10	GND	GND
SO/SIO1	SO/SIO1	8 / 9	WP#/SIO2	WP#/SIO2

8-WSON (8x6mm)				
MX25U25645G	**MX25U25635F**		**MX25U25635F**	**MX25U25645G**
CS#	CS#	1 / 8	VCC	VCC
SO/SIO1	SO/SIO1	2 / 7	RESET#/SIO3	RESET#/SIO3
WP#/SIO2	WP#/SIO2	3 / 6	SCLK	SCLK
GND	GND	4 / 5	SI/SIO0	SI/SIO0

3. Command Set

The core commands for read, erase, and program are unchanged between the F and G versions. For a full list of commands and a description of their functions, please refer to each product's datasheet.

Table 3-1: Command Set Comparison (Read/Erase/Program/ID Read)

Command	Symbol	Description	MX25U25635F	MX25U25645G
Read	READ	Normal Read (1-1-1)	03h	03h
	FASTREAD	Fast Read (1-1-1)	0Bh	0Bh
	DREAD	Dual Output (1-1-2)	3Bh	3Bh
	2READ	2 I/O (1-2-2)	BBh	BBh
	QREAD	Quad Output (1-1-4)	6Bh	6Bh
	4READ	4 I/O (1-4-4, start from bottom 128Mb)	EBh	EBh
	4READ	4 I/O (1-4-4, start from Top 128Mb)	EAh	-
	4DTRD	Quad I/O DT Read	-	EDh
Erase	SE	Sector Erase (4KB)	20h	20h
	BE32KB	Block Erase (32KB)	52h	52h
	BE	Block Erase (64KB)	D8h	D8h
	CE	Chip Erase	60h or C7h	60h or C7h
Program	PP	Page Program	02h	02h
	4PP	Quad Input Page Program	38h	38h
SFDP	RDSFDP	Read SFDP Table	5Ah	5Ah
ID Read	RDID	Read ID	9Fh	9Fh
	RES	Read Electronic ID	ABh	ABh
	REMS	Read Electronic & Manufacturer ID	90h	90h
	QPIID	QPI ID Read	AFh	AFh

Table 3-1: Command Set Comparison (Register/Mode/Reset)

Command	Symbol	Description	MX25U25635F	MX25U25645G
Register	RDSR	Read Status Register	05h	05h
	RDCR	Read Configuration register	15h	15h
	WRSR	Write Status Register	01h	01h
	RDSCUR	Read Security Register	2Bh	2Bh
	WRSCUR	Write Security Register	2Fh	2Fh
	RDFBR	Read Fast Boot Register	16h	16h
	WRFBR	Write Fast Boot Register	17h	17h
	ESFBR	Erase Fast Boot Register	18h	18h
Mode	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	EQIO	Enable QPI	35h	35h
	RSTQIO	Disable QPI	F5h	F5h
	SBL	Set Burst Length	C0h	C0h
	WPSEL	Write Protect Selection	-	68h
	DP	Deep power down	B9h	B9h
	RDP	Release from deep power down	ABh	ABh
	ENSO	Enter Secured OTP	B1h	B1h
	EXSO	Exit Secured OTP	C1h	C1h
	PGM/ERS Suspend	Suspends Program/Erase	B0h	B0h
	PGM/ERS Resume	Resumes Program/Erase	30h	30h
Reset	NOP	No Operation	00h	00h
	RSTEN	Reset Enable	66h	66h
	RST	Reset Memory	99h	99h

Table 3-1: Command Set Comparison (4-Byte Mode/EAR/4-Byte Command Set)

Command	Symbol	Description	MX25U25635F	MX25U25645G
4-Byte Mode	EN4B	Enter 4-byte Address Mode	B7h	B7h
	EX4B	Exit 4-byte Address Mode	E9h	E9h
EAR	WREAR	Write Extended Address Register	C5h	C5h
	RDEAR	Read Extended Address Register	C8h	C8h
4-Byte Command Set	READ4B	Read Data Bytes Using 4 Bytes Address	13h	13h
	FASTREAD4B	Read Data Bytes at HigherSpeed using 4 Bytes Address	0Ch	0Ch
	DREAD4B	Dual Output Fast Read Using 4 Byte Address	3Ch	3Ch
	2READ4B	Dual Input/Output Fast Read Using 4 Byte Address	BCh	BCh
	QREAD4B	Quad Output Fast Read Using 4 Byte Address	6Ch	6Ch
	4READ4B	Quad Input/Output Fast Read Using 4 Byte Address	ECh	ECh
	SE4B	Sector Erase Using 4 Byte Address	21h	21h
	BE32K4B	Block Erase 32KB Using 4 Byte Address	5Ch	5Ch
	BE4B	Block Erase 64KB Using 4 Byte Address	DCh	DCh
	PP4B	Page Program Using 4 Byte Address	12h	12h
	4PP4B	Quad Page Program Using 4 Byte Address	3Eh	3Eh
	4DTRD4B	Quad I/O DT Read	-	EEh

4. Data Protection

Both F and G version products provide two write protection modes to easily protect sectors from inadvertent changes and will be discussed in more details below.

4-1. BP bit Block Protection

Both Macronix MX25U25635F and MX25U25645G can use BP bits in the Status Register to select groups of memory areas for write protection. All the regions protected by F version can be protected by G version with the identical BP setting. Please refer to the following comparison table.

Table 4-1: Block Protection (BP) Comparison of MX25U25635F and MX25U25645G

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level	
BP3	BP2	BP1	BP0	MX25U25635F	MX25U25645G
0	0	0	0	0 (none)	0 (none)
0	0	0	1	1 (1 block, protected block 511th)	1 (1 block, protected block 511th)
0	0	1	0	2 (2 blocks, protected block 510th-511th)	2 (2 blocks, protected block 510th-511th)
0	0	1	1	3 (4 blocks, protected block 508th-511th)	3 (4 blocks, protected block 508th-511th)
0	1	0	0	4 (8 blocks, protected block 504th-511th)	4 (8 blocks, protected block 504th-511th)
0	1	0	1	5 (16 blocks, protected block 496th-511th)	5 (16 blocks, protected block 496th-511th)
0	1	1	0	6 (32 blocks, protected block 480th-511th)	6 (32 blocks, protected block 480th-511th)
0	1	1	1	7 (64 blocks, protected block 448th-511th)	7 (64 blocks, protected block 448th-511th)
1	0	0	0	8 (128 blocks, protected block 384th-511th)	8 (128 blocks, protected block 384th-511th)
1	0	0	1	9 (256 blocks, protected block 256th-511th)	9 (256 blocks, protected block 256th-511th)
1	0	1	0	10 (512 blocks, protected all)	10 (512 blocks, protected all)
1	0	1	1	11 (512 blocks, protected all)	11 (512 blocks, protected all)
1	1	0	0	12 (512 blocks, protected all)	12 (512 blocks, protected all)
1	1	0	1	13 (512 blocks, protected all)	13 (512 blocks, protected all)
1	1	1	0	14 (512 blocks, protected all)	14 (512 blocks, protected all)
1	1	1	1	15 (512 blocks, protected all)	15 (512 blocks, protected all)

5. Register Comparison

The MX25U25645G Status Register bits are backward compatible with the registers of the MX25U25635F.

Table 5-1: Status Register Comparison

	MX25U25635F	MX25U25645G
bit 0	WIP (write in progress bit)	WIP (write in progress bit)
bit 1	WEL (write enable latch)	WEL (write enable latch)
bit 2	BP0 (level of protected block)	BP0 (level of protected block)
bit 3	BP1 (level of protected block)	BP1 (level of protected block)
bit 4	BP2 (level of protected block)	BP2 (level of protected block)
bit 5	BP3 (level of protected block)	BP3 (level of protected block)
bit 6	QE (Quad Enable)	QE (Quad Enable)
bit 7	SRWD (status register write protect)	SRWD (status register write protect)

Basically, Configuration Register bits on G version are backward compatible with the registers of F version. The G version has added Bit4 for Preamble bit Enable to improve data capture reliability while the flash memory is running in high frequency.

Table 5-2: Configuration Register Comparison

	MX25U25635F	MX25U25645G
bit 0	ODS 0 (output driver strength)	ODS 0 (output driver strength)
bit 1	ODS 1 (output driver strength)	ODS 1 (output driver strength)
bit 2	ODS 2 (output driver strength)	ODS 2 (output driver strength)
bit 3	TB (top/bottom selected)	TB (top/bottom selected)
bit 4	Reserved	PBE (Preamble bit Enable)
bit 5	4 BYTE	4 BYTE
bit 6	DC0 (Dummy cycle 0)	DC0 (Dummy cycle 0)
bit 7	DC1 (Dummy cycle 1)	DC1 (Dummy cycle 1)

The MX25U25645G Security Register bits are backward compatible with the registers of the MX25U25635F. The G version has added Bit7 for WPSEL (Write Protect Selection) to improve data protection feature.

Table 5-3: Security Register Comparison

	MX25U25635F	MX25U25645G
bit 0	Secured OTP indicator bit	Secured OTP indicator bit
bit 1	LDSO (indicate if lock-down)	LDSO (indicate if lock-down)
bit 2	PSB (Program Suspend bit)	PSB (Program Suspend bit)
bit 3	ESB (Erase Suspend bit)	ESB (Erase Suspend bit)
bit 4	Reserved	Reserved
bit 5	P_FAIL	P_FAIL
bit 6	E_FAIL	E_FAIL
bit 7	Reserved	WPSEL

6. Electrical Characteristics

The comparison of DC and AC characteristics are shown in Tables 6-1 and 6-2:

Table 6-1: DC Characteristics

DC Performance		MX25U25635F	MX25U25645G
Active Current	Read (4I/O) (max)	25mA @133MHz 20mA @ 108MHz	22mA @133MHz 18mA @104MHz
	Erase (max)	25mA	40mA
	Program (max)	25mA	40mA
VCC Standby Current (typ)		20uA	20uA
Deep Power Down Current (typ)		1.5uA	3uA

Table 6-2: AC Characteristics

AC Performance			MX25U25635F	MX25U25645G
Erase Time	4KB	typ	45ms	25ms
		max	200ms	400ms
	32KB	typ	200ms	150ms
		max	1000ms	1000ms
	64KB	typ	400ms	250ms
		max	2000ms	1300ms
	Chip Erase	typ	200s	75s
		max	320s	150s
Program Time	Byte	typ	16us	25us
		max	30us	60us
	Page (256-Byte)	typ	1ms	0.15ms
		max	3ms	0.75ms
	Write Status Register	typ	-	-
		max	40ms	40ms
Erase/Program Cycles		typ	100,000	100,000
tCLQV (4I/O)	15pf	max	6ns	4.5ns
	30pf	max	8ns	5ns

7. Memory Organization

The memory and sector architecture of the MX25U25645G flash memory are identical to the MX25U25635F flash memory.

8. Device Identification

The Manufacturer ID and Device ID values of the G version flash memory are identical to the F version flash memory.

Table 8-1: Manufacturer ID & Device ID

ID item		MX25U25635F	MX25U25645G
RDID	Manufacturer ID	C2h	C2h
	Type	25h	25h
	Density	39h	39h
RES	Electronic ID	39h	39h
REMS	Manufacturer ID	C2h	C2h
	Device ID	39h	39h
QPIID	Manufacturer ID	C2h	C2h
	Type	25h	25h
	Density	39h	39h

9. Summary

Generally, the MX25U25645G is backward compatible with the MX25U25635F as it is pin and command compatible with the basic Read/Program/Erase commands.

There may be some differences if special features are used such as DTR mode, Advanced Sector Protection and Password protection.

10. Reference Documents

Table 10-1 shows the datasheet versions used for comparison in this application note. For the most current Macronix specification, please refer to the Macronix Website at http://www.macronix.com

Table 10-1: Datasheet Version

Datasheet	Location	Date Issued	Versions
MX25U25635F	Macronix Website	August 04, 2016	Rev. 1.5
MX25U25645G	Macronix Website	March 03, 2017	Rev 1.1

11. Revision History

Table 11-1: Revision History

Revision No.	Description	Page	Date
Rev. 1	Initial Release	ALL	October 20, 2017

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