Comparing Cypress® S26KL512S with Macronix MX25LM51245G

1. Introduction

This application note compares the Macronix 512Mb 3V OctaFlash MX25LM51245G serial flash and the Cypress® S26KL512S serial flash devices. This document does not provide detailed information on each individual device, but highlights the similarities and differences between them. The comparison covers the general features, performance, packaging, command set, and other parameters.

The information in this document is based on datasheets listed in Section 9. Newer versions of the datasheets may override the contents of this document.

2. Feature Comparison

Both flash device families have similar features and functions as shown in Table 2-1. Significant differences are highlighted in blue.

Table 2-1: Features

Feature	Macronix MX25LM51245G	Cypress S26KL512S
Supply Voltage Range	2.7V ~ 3.6V	2.7V ~ 3.6V
Frequency (max)	133MHz	100MHz
READ (1-1-1) (1)	Yes	-
FAST_READ (1-1-1)(1)	Yes	-
OPI (8-8-8)(1)	Yes, Serial Flash protocol-like	Yes, Parallel flash protocol-like
DTR (Double Transfer Rate)	Yes	Yes
Page Program Size	256B	512B
Sector Size	4KB	4KB
Block Size	64KB	256KB
Security OTP Size	1KB	1KB
Program/Erase Suspend & Resume	Yes	Yes
Burst Mode Read	Yes	Yes
Adjustable Output Driver	Yes	Yes
FastBoot Mode	Yes	-
Configurable Dummy Cycles	Yes	Yes
S/W Reset Command	Yes	Yes
RESET# Pin	Yes	Yes
Advanced Sector Protection	Yes	Yes
Manufacturer ID	C2h	0001h
Device ID	85h/3Ah	007Eh/006Fh
Package	16pin SOP 24-BGA (5x5 ball)	24-BGA (5x5 ball)

Note:

1. x-y-z in I/O mode indicates the number of active pins used for op-code(x), address(y) and data(z).

3. Performance Comparison

Tables 3-1 and 3-2 show MX25LM51245G and S26KL512S AC performance.

Table 3-1: Read Performance

Parameter		Macronix MX25LM51245G	Cypress S26KL512S
Normal Read		66MHz	-
Fast Read	1-1-1	133MHz(1)	-
OPI STR Read	8-8-8	133MHz	-
OPI DTR Read	8-8-8 DTR	133MHz(2)	100MHz
tCLQV/ tCKD	30pF	5ns	-
	20pF	5ns	5.5ns
	15pF	5ns	-
	10pF	5ns	-
tDQSQ/ tDSS	30pF	1ns	-
	20pF	0.8ns	0.8ns
	15pF	0.6ns	-
	10pF	0.4ns	-
tQHS/ tDSH	30pF	1.2ns	-
	20pF	1ns	0.8ns
	15pF	0.8ns	-
	10pF	0.6ns	-

Note:

1. MX25LM51245G *Fast Read runs up to 133MHz with default dummy cycles.*
2. MX25LM51245G *OPI runs up to 133MHz with 20 dummy cycles and 104MHz with 10 dummy cycles.*
3. *All values in Table 3-1 are maximum value.*

Table 3-2: Write Performance

Parameter		Macronix MX25LM51245G	Cypress S26KL512S
Erase	4KB	25ms(typ) / 400ms(max)	240ms(typ) / 725ms(max)
	64KB	0.22s(typ) / 2s(max)	-
	256KB	-	0.93s(typ) / 2.9s(max)
Chip Erase / Bulk Erase		150s(typ) / 300s(max)	150s(typ) / 300s(max)
Program	Word	-	0.5ms(typ) / 1.26ms(max)
	Page	0.15ms(256B)(typ) / 0.75ms(max)	0.475ms(512B)(typ) / 2.0ms(max)
Program/Erase Cycles (Endurance)		100,000	100,000

4. DC Characteristics

Both flash series characteristics are similar in primary features and functions. However, there are minor differences in DC characteristics which should be evaluated to determine their significance.

Table 4-1: Read / Write Current

Parameter	Macronix MX25LM51245G	Cypress S26KL512S
Read Current @ OPI	50mA @ 133MHz STR 60mA @ 133MHz DTR	100mA @ 100MHz DTR - VCC 100mA @ 100MHz DTR - VCCQ
Standby Current	180uA	100uA
Deep Power Down Current	80uA @ -40°C ~ 85°C	18uA @ 25°C / 50uA @ 85°C
Write Current	40mA	100mA

Note: All values in Table 4-1 are maximum value.

Table 4-2 compares I/O voltage levels between the two families. Cypress® supports a Versatile I/O Voltage while Macronix does not.

Table 4-2: Input / Output Voltage

Parameter	Macronix MX25LM51245G	Cypress S26KL512S(1)
Input Low Voltage (VIL)	-0.4V (min.) / 0.3VCC (max.)	-0.5V (min.) / 0.3VCC (max.)
Input High Voltage (VIH)	0.7VCC (min.) / VCC+0.4V (max.)	0.7VCC (min.) / VCC+0.3V (max.)
Output Low Voltage (VOL)	0.2V (max.)	0.15V (max.)
Output High Voltage (VOH)	VCC-0.2 (min.)	0.85VCC (min.)

Note:

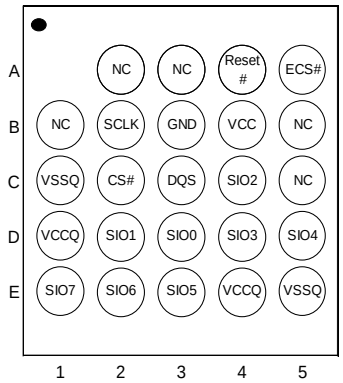
*1. S26KL5122S disclose this value in document HyperBus™ Specification Low Signal Count, High Performance DDR Bus. Document number: 001-99253 Rev. *F*

5. Hardware Consideration

Devices are pin compatible. The MX25LM51245G provides an ECS#(A5) output signal to feedback the ECC correction status, but it is a INT# pin on the S26KL512S. The S26KL512S has a differential a RSTO# ball A2 not provided on the MX25LM51245G (this pin is NC (no connect) on the Macronix flash).

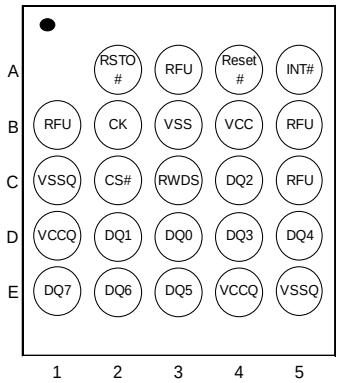
24-BGA (5x5 ball)

MX25LM51245G



Reset# signal is internal pull high

S26KL512S



Reset# signal is internal pull high

Table 5-1: 24-BGA Package Ball Different Definition Comparison

Ball	Macronix MX25LM51245G	Cypress S26KL512S
A2	NC(1)	RTSO#(2)
A3	NC	RFU(1), must be floating or pulled high
A4	ECS#(3)	INT#(4)
B1	NC	RFU
B5/C5	NC	RFU, recommend to be connected to Vss
C3	DQS(5)	RWDS(5)

Note:

1. NC = No Connect; RFU = Reserved for Future Use

2. RTSO# = indicate when a POR is occurring within the device and can be used as a system level reset signal

3. ECS# = ECC Correction Signal

4. INT# = indicate to the host system that an event has occurred within the flash device

5. DQS# = Data Strobe Signal; RWDS = Read Write Data Strobe

During high frequency access, the time scale may become compressed (as compared with traditional Serial NOR flash) resulting in reduced timing margin. The MX25LM51245G has both an SCLK pin and a DQS pin to control data output synchronously at high speed. Systems which only use the SCLK pin to latch data output, may not have enough timing margin to latch data in specific clock cycle under high frequency. S26KL512S uses CK pin with RWDS pin C3 combination to control data output timing. Both devices adapt different methods of supporting stable and valid data for MCU to access flash data under high frequency operation

6. Octa I/O Protocol and High Frequency

Both devices support an Octa I/O interface with low latency access. However, they use different protocols to implement Octa I/O functionality and achieve high frequency operation. In systems which implement an Octa I/O interface, it is necessary to modify H/W and S/W algorithms to achieve Octa I/O operation.

6-1. Octa I/O

MX25LM51245G OctaFlash support Single I/O (x1) mode for backward compatibility, and support Octa I/O mode (x8) to significantly reduce flash access time and throughput. Both modes use a serial flash protocol to reduce system H/W and S/W design effort.

The S26KL512S device supports Octa I/O mode only. Because it doesn't support a serial flash protocol it may require more time to revise the command sequence, increasing system design time. Not only is new command protocol verification needed, but also H/W and S/W implementation will require changes.

6-2. Software Considerations

MX25LM51245G basic command set and 4-Byte command set follow a serial flash command protocol in STR x1 operation. A CMD/CMD# protocol is needed in STR/DTR x8 operation. In comparison, the MX25LM51245G device uses serial flash traditional command protocol for migration purpose. In S26KL512S, it uses parallel flash like command protocol which shows from Table 6-6 to 6-9. Algorithm modifications are necessary to access both flash devices on the application. The most common commands are shown in Tables 6-1 to 6-9.

Table 6-1: MX25LM51245G Basic SPI Command Set (x1)

Instruction Type	Instruction	Description	Op-code
	Macronix MX25LM51245G		Macronix MX25LM51245G
Read	READ3B	Normal Read	03h
	FAST_READ3B	Fast Read (1-1-1)	0Bh
Write	WREN	Write Enable	06h
	WRDI	Write Disable	04h
	PP3B	Page Program	02h
	SE3B	Sector Erase	20h
	BE3B	Block Erase 64KB	D8h
	CE	Chip Erase / Bulk Erase	60h/C7h
	ENSO	Enter Secured OTP	B1h
	EXSO	Exit Secured OTP	C1h
Read ID	RDID	Read Identification	9Fh
Register	RDSR	Read Status Register	05h
	WRSR	Write Status Registers	01h
	WRCR	Write Configuration Registers	01h
	RDCR	Read Configuration Register	15h
	RDCR2	Read Configuration Register2	71h
	WRCR2	Write Configuration Register2	72h
	RDSCUR	Read Security Register	2Bh
	WRSCUR	Write Security Register	2Fh
	ESFBR	Erase Fast Boot Register	18h
	RDFBR	Read FastBoot Register	16h
	WRFBR	Write FastBoot Register	17h

Table 6-2: MX25LM51245G 4-Byte Address SPI Command Set (x1)

Instruction Type	Instruction	Description	Op-code
	Macronix MX25LM51245G		Macronix MX25LM51245G
Read	READ4B	Normal Read	13h
	FAST_READ4B	Fast Read (1-1-1)	0Ch
Write	PP4B	Page Program (1-1-1)	12h
	SE4B	Sector Erase	21h
	BE4B	Block Erase 64KB/256KB	DCh

Table 6-3: MX25LM51245G Other SPI Command Set (x1)

Instruction Type	Instruction	Description	Op-code
	Macronix MX25LM51245G		Macronix MX25LM51245G
Other	SBL	Set Burst Length	C0h
	RSTEN	Reset Enable	66h
	RST	Software Reset Memory	99h
	NOP	No Operation	00h
	PGM/ERS Suspend	Program/Erase Suspend	B0h
	PGM/ERS Resume	Program/Erase Resume	30h
	RDSFDP	Read SFDP	5Ah
	DP	Deep Power Down	B9h

Table 6-4: MX25LM51245G OPI Basic Command Set (x8)

Instruction Type	Instruction	Description	Op-code
	Macronix MX25LM51245G		Macronix MX25LM51245G
Read	8READ	Octa IO Read	ECh-13h
	8DTRD	Octa IO DT Read	EEh-11h
Write	WREN	Write Enable	06h-F9h
	WRDI	Write Disable	04h-FBh
	PP	Page Program	12h-EDh
	SE	Sector Erase	21h-DEh
	BE	Block Erase 64KB	DCh-23h
	CE	Chip Erase / Bulk Erase	60h-9Fh/C7h-38h
	ENSO	Enter Secured OTP	B1h-4Eh
	EXSO	Exit Secured OTP	C1h-3Eh
Read ID	RDID	Read Identification	9Fh-60h
Register	RDSR	Read Status Register	05h-FAh
	WRSR	Write Status Registers	01h-FEh
	WRCR	Write Configuration Registers	01h-FEh
	RDCR	Read Configuration Register	15h-EAh
	RDCR2	Read Configuration Register2	71h-8Eh
	WRCR2	Write Configuration Register2	72h-8Dh
	RDSCUR	Read Security Register	2Bh-D4h

	WRSCUR	Write Security Register	2Fh-D0h
	ESFBR	Erase Fast Boot Register	18h-E7h
	RDFBR	Read FastBoot Register	16h-E9h
	WRFBR	Write FastBoot Register	17h-E8h

Table 6-5: MX25LM51245G OPI Other Command Set (x8)

Instruction Type	Instruction	Description	Op-code
	Macronix MX25LM51245G		Macronix MX25LM51245G
Other	SBL	Set Burst Length	C0h-3Fh
	RSTEN	Reset Enable	66h-99h
	RST	Software Reset Memory	99h-66h
	NOP	No Operation	00h-FFh
	PGM/ERS Suspend	Program/Erase Suspend	B0h-4Fh
	PGM/ERS Resume	Program/Erase Resume	30h-CFh
	RDSFDP	Read SFDP	5Ah-A5h
	DP	Deep Power Down	B9h-46h

Table 6-6: S26KL512S Basic Command Set

Basic Command Table of S26KL512S											
Command		Read	Reset/ ASO Exit	Word Program	Write to Buffer	Chip Erase	Sector Erase	Status Register Read	Status Register Clear	Blank Check	Evaluate Erase Status
1st Bus Cycle	Addr	RA	XXX	555h	555h	555h	555h	555h	555h	(SA) 555h	(SA) 555h
	Data	RD	F0h/ FFh	AAh	AAh	AAh	AAh	70h	71h	33h	D0h
2nd Bus Cycle	Addr			2AAh	2AAh	2AAh	2AAh	XXX			
	Data			55h	55h	55h	55h	RD			
3rd Bus Cycle	Addr			555h	SA*1	555h	555h				
	Data			A0h	25h	80h	80h				
4th Bus Cycle	Addr			PA	SA	555h	555h				
	Data			PD*4	WC*2	AAh	AAh				
5th Bus Cycle	Addr				WBL*3	2AAh	2AAh				
	Data				PD	55h	55h				
6th Bus Cycle	Addr				WBL	555h	SA				
	Data				PD	10h	30h				

Note:

1. *SA: Sector Address*
2. *WC: Word Count which count number is N-1*
3. *WBL: Write Buffer Location*
4. *PD: Write Data*

Table 6-7: S26KL512S Basic Command Set - 2

Basic Command Table of S26KL512S								
Command		Program POR Timer Register	Read POR Timer Register	Load Volatile Config Register	Read Volatile Config Register	Program Non-Volatile Config Register	Erase Non-Volatile Config Register	Read Non-Volatile Config Register
1st Bus Cycle	Addr	555h	555h	555h	555h	555h	555h	555h
	Data	AAh	AAh	AAh	AAh	AAh	AAh	AAh
2nd Bus Cycle	Addr	2AAh	2AAh	2AAh	2AAh	2AAh	2AAh	2AAh
	Data	55h	55h	55h	55h	55h	55h	55h
3rd Bus Cycle	Addr	555h	555h	555h	555h	555h	555h	555h
	Data	34h	3Ch	38h	C7h	39h	C8h	C6h
4th Bus Cycle	Addr	XXX	XXX	XXX	XXX	XXX		XXX
	Data	POR Time	RD POR Time	VCR	RD VCR	NVCR		RD NVCR

Table 6-8: S26KL512S Basic Command Set - 3

Basic Command Table of S26KL512S						
Command		Enter Deep Power Down	Load Interrupt Config Register	Read Interrupt Config Register	Load Interrupt Status Register	Read Interrupt Status Register
1st Bus Cycle	555h	555h	555h	555h	555h	555h
	AAh	AAh	AAh	AAh	AAh	AAh
2nd Bus Cycle	2AAh	2AAh	2AAh	2AAh	2AAh	2AAh
	55h	55h	55h	55h	55h	55h
3rd Bus Cycle	555h	XXX	555h	555h	555h	555h
	B9h	B9h	36h	C4h	37h	C5h
4th Bus Cycle	Addr		XXX	XXX	XXX	XXX
	Data		ICR	RD ICR	ISR	RD ISR

Table 6-9: S26KL512S Basic Command Set - 4

Basic Command Table of S26KL512S								
Command		Erase Suspend	Erase Resume	Program Suspend	Program Resume	ID Entry	CFI Enter	ID-CFI Read
1st Bus Cycle	Addr	XXX	XXX	XXX	XXX	555h	(SA) 55h	(SA) RA
	Data	B0h	30h	51h	50h	AAh	98h	RD
2nd Bus Cycle	Addr					2AAh		
	Data					55h		
3rd Bus Cycle	Addr					(SA) 555h		
	Data					90h		

6-3. Page Program Length Alignment

Page Program maximum lengths are different between the MX25LM51245G and the S26KL512S. Software modification is necessary if the longer page program length is being used. The Page Program length should be set to a maximum of 256 bytes and the 1 to 256 bytes to be programmed must fall within the same 256-Byte page boundary. In addition, Macronix recommends that data be written in multiples of 256-byte pages, or at least in multiples of 16-byte aligned chunks, to enhance data reliability.

6-4. Sector Sizes

The MX25LM51245G has uniform 64KB blocks that are each subdivided into sixteen 4KB sectors. The S26KL512S has uniform 256KB sectors and eight 4KB sectors in parameter sectors. Software adjustments are needed to accommodate the smaller blocks provided by the MX25LM51245G. Please refer to the datasheets listed in Section 9 for memory organization details.

6-5. Read Latency

While the Read latency of the MX25LM51245G and S26KL512S in DTR OPI (x8) mode as the same, there are differences when crossing a page boundary. For the S26KL512S, non-page-aligned reads crossing a page boundary may incur a latency from 0 to 7 clock cycles depending on the initial starting address within the page and the dummy cycle setting. The MX25LM51245G has no such limitation.

6-6. Block Protection Mode

The MX25LM51245G use Status Register BP (Block Protect) bits to software write protect areas of memory, but the S26KL512S uses advance protection mode to set sector protection function.

6-7. Advanced Sector Protection Mode

Both device families offer an Advanced Sector Protection mode used to provide volatile and nonvolatile individual sector (or block) protection, but there are differences that need to be accommodated if this feature is used.

6-8. Status Register, Configuration Register, and Security Register

Both devices use registers to configure flash operation modes, but there are some differences that designers need to be aware of as software modifications may be needed. A detailed register comparison is shown in Table 6-10 to 6-13. If a detailed functional description of register bits is required, please refer to the datasheets listed in Section 9.

Table 6-10: Status Register

Register Bit	Macronix MX25LM51245G	Cypress® S26KL512S
Bit0	WIP; 1=write operation	ESTAT; 1=previous Erase successfully
Bit1	WEL; 1=write enable	SLSB; 1=lock error
Bit2	BP0; BP protection	PSSB; 1=program suspend
Bit3	BP1; BP protection	WBASB; 1=write buffer PGM abort
Bit4	BP2; BP protection	PSB; 1=program fail
Bit5	BP3; BP protection	ESB; 1=erase fail
Bit6	Reserved	ESSB; 1=erase suspend
Bit7	Reserved	DRB; 1=ready
Bit8	-	CRCSSB; 1=CRC in Suspension
Bit9 - 15	-	Reserved

Note: Macronix MX25UM51245G Program and Erase Error bits are located in bits 5 and 6 of its Security Register.

Table 6-11: Configuration Register/ Nonvolatile (Volatile) Configuration Register(1)

Register Bit	Macronix MX25LM51245G	Cypress® S26KL512S
Bit0	ODS0; Output driver strength	Burst Length
Bit1	ODS1; Output driver strength	Burst Length
Bit2	ODS2; Output driver strength	RWDS Stall Control; 1=not stall
Bit3	TB; 1=Bottom area protect	Reserved
Bit4	PBE; 1=Preamble bit Enable	DC0; Dummy Cycle
Bit5	Reserved	DC1; Dummy Cycle
Bit6	Reserved	DC2; Dummy Cycle
Bit7	Reserved	DC3; Dummy Cycle
Bit8 - 9	-	Parameter Sector Mapping
Bit10	-	SRR Freeze; Secure Silicon Register lock
Bit11	-	NVCR(VCR) Freeze; Nonvolatile(Volatile) Configuration Register Lock
Bit12 - 14	-	ODS; Output driver strength
Bit15	-	INT# Enable; 1=INT# disable

Note:

1. In Cypress S26SL512S, The placement of the Configuration Register bits are the same in both the Non-Volatile and Volatile Configuration Registers

2. Macronix MX25UM51245G Dummy cycle bits are located in address 200h of Configuration Register 2.

Table 6-12: Security Register/ECC Status Register

Register Bit	Macronix MX25LM51245G	Cypress® S26KL512S
Bit0	Secured OTP; 1=factory lock	ECCD1; 1=ECC disable
Bit1	LDSO; 1=OTP lock down	EECCD; Error in ECC unit data
Bit2	PSB; 1=Program suspend	EECC; Error in ECC
Bit3	ESB; 1=Erase suspend	CB; 1 bit ECC correction
Bit4	Reserved	2BD; 2 bit ECC detection
Bit5	P_FAIL; 1=Program fail	Reserved
Bit6	E_FAIL; 1=Erase fail	Reserved
Bit7	WPSEL; 1=Individual WP	Reserved
Bit8 - 15	-	Reserved

Table 6-13: MX25LM51245G Configuration Register-2

Address	Register Bit	Symbol	Define
00000000h	Bit0	SOPI; STR OPI Enable	00=SPI; 01=STR OPI 10=DTR OPI; 11=inhibit
	Bit1	DOPI; DTR OPI Enable	
	Bit2 – Bit7	Reserved	
00000200h	Bit0	DQSPRC; DTR DQS pre-cycle	1=1 cycle
	Bit1	DOS; DQS on STR mode	1=Enable
	Bit2 – Bit7	Reserved	
00000300h	Bit0 – Bit2	DC; Dummy cycle	
	Bit3 – Bit7	Reserved	
00000500h	Bit0	PPTSEL; Preamable pattern selection	
	Bit1 – Bit7	Reserved	
00000800h	Bit0 – Bit3	ECCCNT; ECC failure chunk counter	
	Bit4 – Bit6	ECCFS; ECC fail status	
	Bit7	ECCFAVLD; ECC fail addr. valid indicator	
00000C00h	Bit0 – Bit3	Reserved	
	Bit4 – Bit7	ECCFA; ECC failure chunk addr.	
00000D00h	Bit0 – Bit7	ECCFA; ECC failure chunk addr	
00000E00h	Bit0 – Bit7	ECCFA; ECC failure chunk addr	
00000F00h	Bit0 – Bit1	ECCFA; ECC failure chunk addr	
	Bit2 – Bit7	Reserved	
40000000h	Bit0	DEFSOPI#; Enable SOPI after power on	00=Inhibit; 01=Default DOPI 10=Default SOPI; 11=SPI
	Bit1	DEFDOPI#; Enable DOPI after power on	
	Bit2 – Bit7	Reserved	
80000000h	Bit0 – Bit3	Reserved	
	Bit4	CRCERR; CMD# or Parity checked fail	
	Bit5 – Bit7	Reserved	

6-9. Manufacturer and Device Identification Numbers

Table 6-14 compares the Manufacturer and Device IDs returned by the RDID commands.

Table 6-14: Manufacturer and Device ID

Command Type	Macronix MX25LM51245G	Cypress® S26KL512S
RDID	C2h/85h/3Ah	0001h/007Eh/006Fh

7. Summary

The Macronix MX25LM51245G OctaFlash and Cypress® S26KL512S both support an Octa I/O interface. Additionally, the supported 24-BGA packages are expected to have similar footprints and nearly identical pin out definitions. Software modification will be needed to accommodate differences in the Octa I/O protocol, differences in status and configuration register bit assignments and the commands used to access them. A more detailed analysis should be done if functions such as Advanced Sector Protection, or DTR are used.

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed specification, please refer to the Macronix Website at: http://www.macronix.com.
Table 8-2 shows the reference document used in this application note.

Table 8-1: Datasheet Version

Datasheet	Location	Data Issued	Version
MX25LM51245G	Website	Nov. 24, 2016	Rev. 1.0
S26KL512S	Website	Aug. 28, 2017	Rev. J

Table 8-2: Reference Document

Title	Location	Data Issued	Version
HyperBus™ Specification Low Signal Count, High Performance DDR Bus	Website	Jun. 13, 2017	Rev. *F

9. Appendix

Table 9-1 shows the basic part number and package information cross reference between Macronix MX25LM51245G and Cypress® S26KL512S parts.

Table 9-1: Part Number Cross Reference

Density	Macronix Part No.	Cypress Part No.	Package	Dimension
512Mb	MX25LM51245GXDI00	S26KL512SDABHI02	24-BGA	5x5 ball

10. Revision History

Revision	Description	Date
1.0	Initial Release	Aug. 25, 2016
2.0	DC/AC parameter, Register value revise	Jan. 03, 2018

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For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com