Comparing Micron® N25Q512A with Macronix MX66U51235F

1. Introduction

This application note serves as a guide to compare the Micron® N25Q512A with the Macronix MX66U51235F 1.8V 512Mb Serial NOR Flash. The document does not provide detailed information on each individual device, but highlights the similarities and differences between them. The comparison covers the general features, performance, command codes, and other differences.

The devices are essentially pin compatible if the HOLD# function is not used. The devices are command compatible for “basic” Read, Program, and Erase commands.

The information provided in this document is based on datasheets listed in Section *"9. References"*. Newer versions of the datasheets may override the contents of this document.

2. Feature Comparison

Both flash device families have similar features and functions as shown in Table 2-1.

Table 2-1: Key Feature Comparison

Type / Function		Micron® N25Q512A	Macronix MX66U51235F
VCC Voltage Range		1.7V-2.0V	1.65V-2.0V
Sector Size		4KB/64KB	4KB/32KB/64KB
Program Buffer Size		256Byte	256Byte
Fast Read Clock Frequency 2x I/O: 8dummy cycles 4x I/O: 8dummy cycles		108MHz(x1) 108MHz(x2) 108MHz(x4)	108MHz(x1) 108MHz(x2) 108MHz(x4)
Fast Read	(1-1-1)	YES	YES
Dual Output (DREAD)	(1-1-2)	YES	YES
Dual I/O (2READ)	(1-2-2)	YES	YES
Dual Peripheral Interface	(2-2-2)	YES	-
Quad Output (QREAD)	(1-1-4)	YES	YES
Quad I/O (4READ)	(1-4-4)	YES	YES
Quad Peripheral Interface (QPI)	(4-4-4)	YES	YES
Normal Read Clock Frequency		54MHz	55MHz
XIP / Performance Enhanced Mode	(1-1-1)	YES	-
	(1-1-2)	YES	-
	(1-2-2)	YES	-
	(2-2-2)	YES	-
	(1-1-4)	YES	-
	(1-4-4)	YES	YES
	(4-4-4)	YES	YES
XIP Mode Set at Power-on		YES	YES
HOLD# / RESET# Pin		Available with either Hold or Reset	Reset only
Security OTP		64Byte	512Byte
Program/Erase Suspend & Resume		YES	YES
Read Enhance Mode		YES	YES
Wrap Around Read Mode		YES	YES
Configurable Dummy Cycles		YES	YES
Adjustable Output Driver		YES	YES
S/W Reset Command		YES	YES
Block Protection Mode		Top/Bottom	Top/Bottom
Individual Sector/Block Protection Mode		YES	-
Program/Erase Cycles		100K	100K

3. Package and Pinout Comparison

The Macronix MX66U51235F and Micron® N25Q512A are available in 16-SOP and 8-WSON packages with identical footprints. Please consult the latest Macronix datasheet for additional package options.

Table 3-1: Packages

Packages	Micron® N25Q512A	Macronix MX66U51235F
8-WSON (8x6mm 3.4 x4.3 EP)	-	YES
8-WSON (8x6mm)	YES	-
16-SOP (300mil)	YES	YES
24-TPBGA (8x6mm)	YES	-

Pinout definitions of the 16-SOP and 8-WSON packages are the same with the exceptions listed in Tables 3-2 and 3-3.

On pin 1 of the 16-SOP package, Macronix has DNU/SIO3, but Micron® has either HOLD#/DQ3 or a RESET#/DQ3. If the Micron® device has RESET#/DQ3, then the devices are pin compatible. If the Micron® device has HOLD#/DQ3, but the HOLD# function is not used or pin 1 is pulled high, then the devices are also pin compatible. If Quad mode is not used, the MX66U51235F DNU/SIO3 pin should be pulled high with a resistor to VCC or left unconnected.

Table 3-2: 16-SOP Pin Definition Comparison Table

16-PIN SOP (300mil)				
Macronix MX66U51235F	**Micron® N25Q512A**		**Macronix MX66U51235F**	**Micron® N25Q512A**
DNU/SIO3	HOLD#/DQ3	1 / 16	SCLK	C
VCC	V_{CC}	2 / 15	SI/SIO0	DQ0
RESET#	DNU	3 / 14	NC	DNU
NC	DNU	4 / 13	NC	DNU
NC	DNU	5 / 12	NC	DNU
NC	DNU	6 / 11	NC	DNU
CS#	S#	7 / 10	GND	V_{ss}
SO/SIO1	DQ1	8 / 9	WP#/SIO2	V_{PP}/DQ2

Table 3-3: 8-WSON Pin Definition Comparison Table

8-WSON (8x6mm 3.4x4.3 EP)				
Macronix MX66U51235F	**Micron® N25Q512A**		**Macronix MX66U51235F**	**Micron® N25Q512A**
CS#	S#	1 / 8	VCC	V_{CC}
SO/SIO1	DQ1	2 / 7	RESET#SIO3	HOLD#/DQ3
WP#/SIO2	V_{PP}/DQ2	3 / 6	SCLK	C
GND	V_{ss}	4 / 5	SI/SIO0	DQ0

4. Key Feature and Operational Differences

This section will describe some of the key features and operational differences in depth.

4-1. Address Protocol Support

Both the Macronix MX66U51235F and the Micron® N25Q512A support three different methods to access the full 512Mb memory space as shown in Table 4-1. There is an important difference between both products. When the Read operation is reaching to 256Mb boundary area, Macronix's product will cross the boundary to another 256Mb die while Micron's product will go back to the beginning of the same 256Mb die. For example, user can read complete device by single command in Macronix's product but need to execute read command twice in Micron's product. In addition, there are slight differences in their implementations which are discussed in the following section.

Table 4-1: 512Mb Address Methods

Address Method	Micron® N25Q512A	Macronix MX66U51235F
4-Byte Mode	YES	YES
Extended Address Register (EAR)	YES	YES
4-Byte Command Set	YES	YES

4-1-1. 4-Byte Mode

4-Byte mode is supported by both products. In 4-Byte mode, the legacy command set is used, but 4-bytes of address are sent during the address phase. Although both Macronix and Micron® support the same command codes to enter and exit 4-Byte Mode, the Macronix EN4B and EX4B commands do not require the WREN command to be issued first. The Macronix MX66U51235F enters 4-Byte mode by using the EN4B command and exits 4-Byte addressing Mode with the EX4B command. A Power-cycle or Reset of the MX66U51235F will also exit 4-Byte mode and return it to the default 3-Byte mode. Table 4-2 shows the status bit settings and commands required to enter and exit 4-Byte addressing mode.

Table 4-2: Related Register: Configuration Register

	Micron® N25Q512A	Macronix MX66U51235F
Related Register	Nonvolatile Configuration Register	Configuration Register
Related Register Bit	Bit [0]- Address bytes	Bit [5]- 4 BYTE
Bit Status	1=Enable 4-Byte Address 0=Enable 3-Byte Address(Default)	1=Enable 4-Byte Address 0=Enable 3-Byte Address(Default)
Enable/Write Command	ENTER 4-BYTE MODE (B7h)	EN4B (B7h)
Disable/Clear Command	EXIT 4-BYTE MODE (E9h)	EX4B (E9h)
WREN	Required	Not Required

4-1-2. Extended Address Register

Both products support an Extended Address Register (EAR). If the system only supports 3-Byte addressing, the Extended Address Register mode is an alternative method that can be used to access memory beyond the 128Mb limit. The EAR supplies the higher address bits to form the starting address for read operations. By setting up the Extended Address register Bit [1:0] (A24, A25), the user can use the original 3-byte address to access both Top and Bottom 128Mb. Please note that the default state of A24 and A25 are “0” in both products, which allows access to the Bottom 128Mb of memory. The WREAR (C5h) command can be used to change the state of A24 and A25 in either device. Both devices need to input the WREN Command before issuing the WREAR command. In addition, both products support the RDEAR (C8h) command to read the state of the EAR bit.

Table 4-3: Related Register: Extended Address Register

	Micron® N25Q512A		Macronix MX66U51235F
Related Register	Nonvolatile Configuration Register	Extended Address Register	Extended Address Register
Related Bit	Bit [1]- 128Mb segment select (only work at 3Byte Address Mode)	Bit [1:0]	Bit [1:0]
Bit Status	0=Top 128Mb segment 1=Bottom 128Mb segment (Default)	Please see Figure 3-1	Please see Figure 3-1
Write Command	WRITE NONVOLATILE CONFIGURATION REGISTER (B1h)	WRITE EXTENDED ADDRESS REGISTER (C5h)	WREAR (C5h)
Read Command	READ NONVOLATILE CONFIGURATION REGISTER command (B1h)	READ EXTENDED ADDRESS REGISTER (C8h)	RDEAR (C8h)
WREN	Required	Required	Required

Figure 3-1: EAR Operation Segments

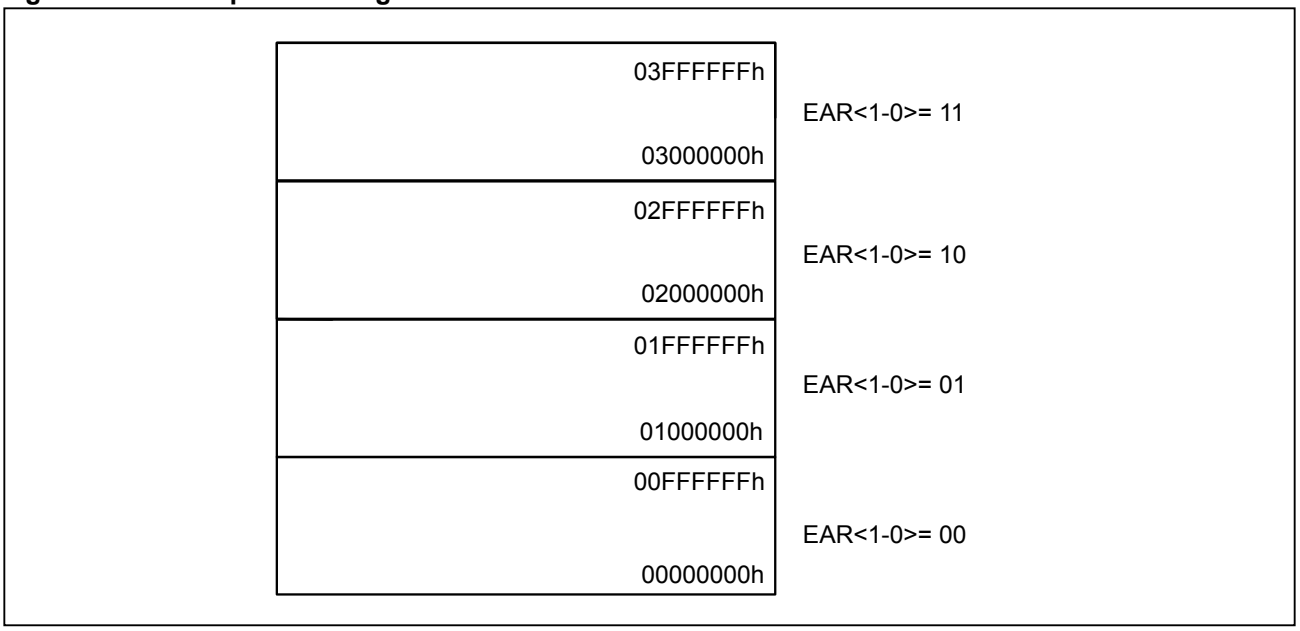

Table 4-4: Extended Address Register Bits

Micron® N25Q512A -Extended Address Register				MX66U51235F -Extended Address Register			
Bits	Description	Default Status	Type	Bits	Description	Default Status	Type
Bit 7	A[31:26]; Reserved		volatile	Bit 7	A31	0	volatile
Bit 6			volatile	Bit 6	A30	0	volatile
Bit 5			volatile	Bit 5	A29	0	volatile
Bit 4			volatile	Bit 4	A28	0	volatile
Bit 3			volatile	Bit 3	A27	0	volatile
Bit 2			volatile	Bit 2	A26	0	volatile
Bit 1	A25	0	volatile	Bit 1	A25	0	volatile
Bit 0	A24	0	volatile	Bit 0	A24	0	volatile

4-1-3. 4-Byte Command Set

The MX66U51235F and Micron® N25Q512A have additional new commands for 4-byte addressing. The operation of 4-byte address command sets are very similar to the original 3-byte address command sets. The only difference is that all of the 4-byte address commands require that the instruction code be followed by 4-bytes of address (A31-A0). The 4-Byte address command set eliminates the need to enter or exit 4-Byte addressing mode.

Table 4-5: 4-Byte Command Set

	Instruction	Description	Micron® N25Q512A	Macronix MX66U51235F
4-Byte Command Set	READ4B	Read Data Bytes	13h	13h
	FAST_READ4B	Read Data Bytes at Higher Speed	0Ch	0Ch
	DREAD4B	Dual Output Fast Read	3Ch	3Ch
	2READ4B	Dual Input/Output Fast Read	BCh	BCh
	QREAD4B	Quad Output Fast Read	6Ch	6Ch
	4READ4B	Quad Input/Output Fast Read	ECh	ECh
	PP4B	Page Program	-	12h
	4PP4B	Quad Page Program (1-1-4)	-	3Eh
	SE4B	Sector Erase	-	21h
	BE4B	Block Erase 64KB	-	DCh
	BE32K4B	Block Erase 32KB	-	5Ch

4-2. Status Register BP Protection Differences

Both the Micron® and Macronix devices use BP[3:0] bits to select similar memory areas for protection.

The Micron® N25Q512A Block Protection bits BP[3:0] are located in Status Register (bits 6 and [4:2]). The Top/Bottom bit is located in Status Register bit 5 and selects whether block protection starts at the top or bottom of memory. The BP[3:0] and Top/Bottom bits are nonvolatile and reprogrammable.

The MX66U51235F Block Protection bits BP[3:0] are located in Status Register bits [5:2]. The top/bottom starting point is controlled by the TB bit, which is located in Configuration Register bit 3. The default setting of the TB bit starts block protection at the top of memory. If the 'bottom' starting point is selected, it can never be returned to the 'top' starting point. The BP[3:0] bits are all nonvolatile and reprogrammable. The TB bit is nonvolatile and one-time-programmable.

4-3. Individual Sector/Block Protection Differences

The Micron® N25Q512A has the ability to protect individual 64KB sectors/blocks of memory independent of the nonvolatile BP bit configuration in the Status Register.

The MX66U51235F does not support Individual Sector/Block Protection function.

4-4. QPI Differences

Micron®'s Quad I/O mode is entered by setting a bit in the Nonvolatile Configuration Register, which remembers this mode after power cycles, or by setting a bit in the Enhanced Volatile Configuration Register and is reset after a power cycle.

The MX66U51235F requires an EQIO (35h) command to enter the equivalent QPI mode. This mode can be terminated by a RSTQIO (F5h) command, a power cycle, hardware reset, or software reset. (Please note that on the 8-WSON package, hardware RESET# is disabled during QPI or Quad mode).

4-5. XIP Differences

The XIP (eXecute In Place) feature (Macronix refers to this as Performance Enhance Mode) is only used during Fast Read operations and eliminates the need to input read commands prior to entering an address and reading data. This is an overhead reduction feature that reduces data latency. Both devices offer this feature, but entry and exit methods are different and not all I/O modes are supported by Macronix. As can be seen in *"Table 2-1: Key Feature Comparison"* above, Macronix only supports XIP in Quad I/O (1-4-4) and QPI (4-4-4) modes. Micron® supports XIP in all Fast Read I/O modes.

4-5-1. Entering XIP Mode

The Micron® N25Q512A can be configured to power-up in any XIP mode or entered later using the Volatile Configuration Register (depends on feature set selected by part number) and/or setting the XIP confirm bit to '0' (first dummy cycle bit on DQ0 of any Fast Read command). The MX66U51235F enters XIP mode whenever all four bits of the first and second dummy cycles of a 4READ instruction are not equal.

4-5-2. Exiting XIP Mode

The Micron® N25Q512A will automatically exit XIP mode after the current read operation if the XIP confirm bit is not '0' (first dummy cycle bit on DQ0). The MX66U51235F will exit XIP mode if any of the bits of the first and second dummy cycles are equal. In 3-byte addressing mode, this can be accomplished by sending command FFh or 00h on SIO0 (SPI mode) and FFFFFFFFh (QPI mode). In 4-byte addressing, it can be accomplished by sending command 3FFh on SIO0 (SPI mode) and FFFFFFFFFFh (QPI mode).

4-6. Status Register and Configuration Register Differences

Both devices use status and configuration registers to control device behavior and report status. The registers and bits used are not identical. Please refer to the datasheets to compare register definitions and usages.

4-7. Chip Read and Erase Differences

The Micron N25Q512A only supports the Die Erase function, which means users have to execute two Die Erase Commands (once in each die) to finish a chip erase operation. In the meantime, The Macronix MX66U51235F device looks and works like a monolithic 512Mb die and only need one CE command with no address required.

Similarly, because Micron treats its two die solution as two independently addressable arrays, extra steps may be required when using the Micron flash during Reads which are not required for the Macronix flash. For example, per the Micron datasheet "After any READ command is executed, the device will output data from the selected address in the die. After a die boundary is reached, the device will start reading again from the beginning of the same 256Mb die. A complete device reading is completed by executing read twice." Macronix has no such requirement: "the whole memory can be read out with a single READ instruction. The address counter rolls over to 0 when the highest address has been reached."

5. Performance Comparison

Tables 5-1 and 5-2 show that the two devices have similar AC and DC performance.

Table 5-1: AC Parameter Comparison

Parameter	Symbol		Condition	Micron® N25Q512A	Macronix MX66U51235F
	Micron®	Macronix			
Clock High Time	tCH	tCH	min	4ns	4.5
Clock Low Time	tCL	tCL	min	4ns	4.5
Clock Low to Output Valid	tCLQV	tCLQV	max @10pF	5ns	-
			max @15pF	-	9ns
			max @30pF	7ns	12ns
Data In Setup Time	tDVCH	tDVCH	min	2ns	2.5ns
Data In Hold Time	tCHDX	tCHDX	min	3ns	3.5ns
Page Program Time (256 Bytes)	tPP	tPP	typ	0.5ms	1.2ms
			max	5ms	3ms
Erase 4KB Subsector/ Sector	tSSE	tSE	typ	250ms	60ms
			max	0.8s	0.2s
Erase 32KB Sector	-	tBE32	typ	-	0.25s
			max	-	1s
Erase 64KB Sector/Block	tSE	tBE	typ	0.7s	0.5s
			max	3s	2s
Die Erase	tBE	-	typ	240s	-
			max	480s	-
Chip Erase	-	tCE	typ	-	200s
			max	-	320s

Table 5-2: DC Parameter Comparison

Parameter	Symbol		Condition	Micron® N25Q512A	Macronix MX66U51235F
	Micron®	Macronix			
Leakage Current	ILI/ILO	ILI/ILO	max	+/- 2uA	+/- 4uA
Standby Current	ICC1	ISB1	typ	-	60uA
			max	150uA	200uA
Deep Power Down Current	-	ISB2	typ	-	10uA
			max	-	40uA
VCC Read Current (Fast Read)	ICC3	ICC1	max @ 108MHz (4-4-4)	20mA	40mA
			max @ 84MHz	-	30mA
			max @ 54MHz	6mA	-
VCC Program Current	ICC4	ICC2	max	20mA	25mA
VCC Write Status Register Current	ICC5	ICC3	max	20mA	40mA
VCC Erase Current (Except Macronix Chip Erase Current)	ICC6	ICC4	max	20mA	25mA
VCC Chip Erase Current	-	ICC5	max	-	50mA

6. Command Code Comparison

Both devices use similar basic command set, but there are a few minor differences highlighted in Table 6-1. For 4-byte address command set, please refer to *"Table 4-5: 4-Byte Command Set"*.

Table 6-1: Command Code Comparison

Instruction Type	Instruction	Description	Micron® N25Q512A	Macronix MX66U51235F
Read ID	RDID	Read Identification	9Eh/9Fh	9Fh
	REMS	Read Electronic Manufacturer ID & Signature	-	90h
Read	READ	Read Data Bytes	03h	03h
	FAST_READ	Read Data Bytes at Higher Speed	0Bh	0Bh
	DOFR	Dual Output Fast Read	3Bh	3Bh
	DIOFR	Dual Input/Output Fast Read	BBh	BBh
	QOFR	Quad Output Fast Read	6Bh	6Bh
	QIOFR	Quad Input/Output Fast Read	EBh	EBh
	RDSFDP	Read Serial Flash Discoverable Parameters	5Ah	5Ah
Write	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	PP	Page Program	02h	02h
	-	Dual Input Fast Program (1-1-2)	A2h	-
	-	Quad Input Fast Program (1-1-4)	32h	-
	4PP	Quad Page Program (1-4-4)	12h	38h
	SE	Sector Erase 4KB	20h	20h
	BE 32K	Block Erase 32KB	-	52h
	SE 64K	Block Erase 64KB	D8h	D8h
	BE	Die Erase (256Mb)	C4h	-
	CE	Chip Erase (512Mb)	-	60 or C7h
Register	RDSR	Read Status Register	05h	05h
	RDCR	Read Configuration Register	-	15h
	WRSR	Write Status Register	01h	01h
	RDSCUR	Read Security Register	-	2Bh
	WRSCUR	Write Security Register	-	2Fh
	RDLR	Read Lock Register	E8h	-
	WRLR	Write Lock Register	E5h	-
	RFSR	Read Flag Status Register	70h	-
	CLFSR	Clear Flag Status Register	50h	-
	-	Read Non-volatile Configuration Register	B5h	-
	-	Write Non-volatile Configuration Register	B1h	-
	-	Read Volatile Configuration Register	85h	-
	-	Write Volatile Configuration Register	81h	-
	-	Read Enhance Volatile Configuration Register	65h	-
	-	Write Enhance Volatile Configuration Register	61h	-

Table 6-1: Command Code Comparison - Continued

Instruction Type	Instruction	Description	Micron® N25Q512A	Macronix MX66U51235F
QPI	EQIO	Enable QPI	-	35h
	RSTQIO	Reset (Exit) QPI	-	F5h
	QPIID	QPI ID Read	AFh	AFh
OTP	ENSO	Enter Secured OTP	-	B1h
	EXSO	Exit Secured OTP	-	C1h
	ROTP	Read OTP Area	4Bh	-
	POTP	Program OTP Area	42h	-
Others	PGM/ERS Suspend	Program or Erase Suspend	75h	B0h
	PGM/ERS Resume	Program or Erase Resume	7Ah	30h
	RSTEN	Reset Enable	66h	66h
	RST	Reset Memory	99h	99h
	SBL (1)	Set Burst Length	-	C0h
	NOP	No Operation	-	00h
	DP	Deep Power Down	B9h	B9h
	RDP	Release From Deep Power Down	ABh	ABh
	-	Release Read Enhanced	-	FFh

Note 1: Micron® uses the Volatile Configuration Register to control the Set Burst Length function.

7. Manufacturer and Device ID Comparison

Table 7-1: Manufacturer and Device ID Comparison

Name		Micron® N25Q512A	Macronix MX66U51235F
Manufacture ID		20h	C2h
Device ID	Memory Type	BBh	25h
	Memory Capacity	20h	3Ah
Unique ID		17 Bytes	N/A

8. Summary

The Macronix MX66U51235F and Micron® N25Q512A have similar commands, functions, and features. The devices are essentially pin compatible if the HOLD# function is not used. A more detailed analysis should be done if “special” functions such as Chip Erase, XIP, Individual Sector Write Protection, or Dual I/O (2-2-2) are used.

9. References

Table 9-1 shows the datasheet versions used for comparison in this application note. For the most current, detailed Macronix specification, please refer to the Macronix Website at http://www.macronix.com/.

Table 9-1: Datasheet Version

Datasheet	Location	Date Issued	Version
MX66U51235F	-	SEP. 2013	0.01
Micron® N25Q512A	Micron® Website	MAY. 2013	I

10. Revision History

Revision No.	Description	Page	Date
Rev. 1	Initial Release	ALL	September 13, 2013
Rev. 2	1. Title and description modification. 2. Added "Macronix Proprietary" footnote.	ALL	January 17, 2018

Except for customized products which have been expressly identified in the applicable agreement, Macronix's products are designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and not for use in any applications which may, directly or indirectly, cause death, personal injury, or severe property damages. In the event Macronix products are used in contradicted to their target usage above, the buyer shall take any and all actions to ensure said Macronix's product qualified for its actual use in accordance with the applicable laws and regulations; and Macronix as well as it's suppliers and/or distributors shall be released from any and all liability arisen therefrom.

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