The Comparison of MX25L12835F/33F/73F and MX25L12872F

1. Introduction

This application note compares Macronix MX25L12835F/33F/73F and MX25L12872F Serial NOR Flash products. The document does not provide detailed information on individual devices, but highlights the similarities and differences between them. The comparison covers the general features, performance, command sets, and device identification numbers.

The information provided in this document is based on datasheets listed in Section *8. References*. Newer versions of the datasheets may override the contents of this document.

2. General Features

2-1. Feature Comparison

The MX25L12872F product provides a feature rich solution to cover legacy products including MX25L12835F/33F/73F.

The Configuration Register sets the number of dummy clock cycles used for fast read operations, the output drive strength, and selects either the top or bottom of memory to be a Block Protect (BP) area.

The MX25L12835F/33F/73F and MX25L12872F devices support an individual block protection method as an alternative to the grouped block protection provided by Status Register Block Protection (BP) bits. In addition, all of them have added additional protection features in the Advanced Sector Protection mode that provide higher levels of protection. These higher levels of protection include:

1. Nonvolatile individual sector/block protection.
2. A software locking mechanism to prevent modifications to the nonvolatile protection until the next reset cycle or power-up cycle.
3. A password protection cycle (only provided by MX25L12835F/73F).

These additional protection features can be used to prevent accidental or deliberate data corruption in protected memory areas.

For the comparisons of MX25L12835F/33F/73F and MX25L12872F, the differences are listed as below:

1. Secured OTP: Both MX25L12833F and MX25L12872F have additional 8K-bit secured OTP mode, while MX25L12835F/73F have 4K-bit secured OTP mode.
2. Fast Boot Mode: The fast boot mode is only provided by MX25L12835F/73F.
3. Password Protection: The password protection is only provided by MX25L12835F/73F.
4. The Quad I/O mode is permanently enabled on MX25L12873F and MX25L12872F.

Please refer to the MX25L12835F/33F/73F and MX25L12872F datasheets for more details.

For additional product differences, please refer to the descriptions and comparison tables below.

Table 2-1. Feature Comparison

Part no.		MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
Technology		75nm	75nm	75nm	75nm
Density		128Mb	128Mb	128Mb	128Mb
VCC		2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Structure					
Fast Read I/O Support	FAST READ (1-1-1)	Yes	Yes	Yes	Yes
	DREAD (1-1-2)	Yes	Yes	Yes	Yes
	2READ (1-2-2)	Yes	Yes	Yes	Yes
	QREAD (1-1-4)	Yes	Yes	Yes	Yes
	4READ (1-4-4)	Yes	Yes	Yes	Yes
	QPI (4-4-4)	Yes	Yes	Yes	Yes
DTR		-	-	-	-
Configurable Dummy Cycles		Yes	Yes	Yes	Yes
Sector Size		4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB	4KB/32KB/64KB
Program Buffer Size		256Byte	256Byte	256Byte	256Byte
Secured OTP		4Kb	8Kb	4Kbit	8Kbit
BP Protect		Top/Bottom	Top/Bottom	Top/Bottom	Top/Bottom
4 I/O Mode Permanently Enabled		-	-	Yes	Yes
Software Features					
Read Enhance Mode		Yes	Yes	Yes	Yes
Wrap-around Read Mode		Yes	Yes	Yes	Yes
S/W Reset Command		Yes	Yes	Yes	Yes
Erase Suspend & Resume		Yes	Yes	Yes	Yes
Program Suspend & Resume		Yes	Yes	Yes	Yes
Adjustable Output Driver Strength		Yes	Yes	Yes	Yes
Fast Boot Mode		Yes	-	Yes	-
Deep Power Down		Yes	Yes	Yes	Yes
Individual/Volatile Write Protection		Yes	Yes	Yes	Yes
Individual/Nonvolatile Write Protection		Yes	Yes	Yes	Yes
Password Protection		Yes	-	Yes	-
Hardware Features					
Reset# Pin		Yes	Yes	-	-
Hold# Pin		-	-	-	-
Package Solution	8SOP (209mil)	Yes	Yes	Yes	Yes
	16SOP (300mil)	Yes	Yes	Yes	-
	8WSON (8x6mm^2)	Yes	Yes	-	-
	8WSON (6x5mm^2)	Yes	Yes	Yes	Yes

2-2. Write Protection Comparison

The MX25L12835F/33F/73F and MX25L12872F products provide two write protection modes to easily protect sectors from inadvertent changes.

The default is Block Protection Mode, utilizing the nonvolatile Block Protection (BP) bits in the Status Register. The BP bits specify which block groups will be protected.

The second mode uses an individual block protection method. This method utilizes a volatile SRAM lock bit assigned to each block (or sector) and controls its protection status. The Gang Block Lock (GBLK) and Gang Block Unlock (GBULK) commands set or clear all SRAM lock bits simultaneously.

2-2-1 Block Protection (BP) Mode

The MX25L12835F/33F/73F and MX25L12872F use identical Status Register BP bits to specify which group of blocks to be protected; they have a finer granularity of protection and have the ability to specify whether block protection begins at the top or bottom of memory. This is controlled by the Top/Bottom (TB) bit in the Configuration Register. The TB default setting is '0' and specifies the top of the memory as shown in **Table 2-2** and *Table 2-3: Block Protection (BP) Comparison (Bottom memory blocks)*.

Table 2-2: Block Protection (BP) Comparison (Top memory blocks)

Status Register Bit				Protected Blocks	
BP3	BP2	BP1	BP0	**MX25L12835F/33F/73F** **MX25L12872F**	
0	0	0	0	None	
0	0	0	1	1 block	(#255)
0	0	1	0	2 blocks	(#254-255)
0	0	1	1	4 blocks	(#252-255)
0	1	0	0	8 blocks	(#248-255)
0	1	0	1	16 blocks	(#240-255)
0	1	1	0	32 blocks	(#224-255)
0	1	1	1	64 blocks	(#192-255)
1	0	0	0	128 blocks	(#128-255)
1	0	0	1	256 blocks	(all)
1	0	1	0	256 blocks	(all)
1	0	1	1	256 blocks	(all)
1	1	0	0	256 blocks	(all)
1	1	0	1	256 blocks	(all)
1	1	1	0	256 blocks	(all)
1	1	1	1	256 blocks	(all)

Table 2-3: Block Protection (BP) Comparison (Bottom memory blocks)

Status Register Bit				Protected Blocks	
BP3	BP2	BP1	BP0	**MX25L12835F/33F/73F** **MX25L12872F**	
0	0	0	0	None	
0	0	0	1	1 block	(#0)
0	0	1	0	2 blocks	(#0-1)
0	0	1	1	4 blocks	(#0-3)
0	1	0	0	8 blocks	(#0-7)
0	1	0	1	16 blocks	(#0-15)
0	1	1	0	32 blocks	(#0-31)
0	1	1	1	64 blocks	(#0-63)
1	0	0	0	128 blocks	(#0-127)
1	0	0	1	256 blocks	(all)
1	0	1	0	256 blocks	(all)
1	0	1	1	256 blocks	(all)
1	1	0	0	256 blocks	(all)
1	1	0	1	256 blocks	(all)
1	1	1	0	256 blocks	(all)
1	1	1	1	256 blocks	(all)

2-2-2 Individual Block Protection Mode

Individual block protection is only effective after executing the WPSEL command. This one-time-use command permanently disables the block group protection method (Status Register BP bits) and activates individual block protection. The Individual Block Protection Mode is also called Advanced Sectore Protection.

2-2-3 MX25L12835F/33F/73F and MX25L12872F Individual Block Protection Mode

Dynamic Protection Bits (DPB) is volatile and similar in purpose to the Single Block Lock Protection bits. Nonvolatile Solid Protection Bits (SPB) is a new feature. Each protectable sector or block is assigned one DPB and one SPB. This permits sector or block protection to be specified individually and independent of any other sector or block. The DPB default to the protect state (FFh) upon power-up or reset. They work in conjunction with the nonvolatile SPB. Both DPB and SPB states must be cleared to 00h before the associated sector or block can be modified, and the SPB are preset to 00h at the factory. Please refer to the datasheet of MX25L12835F/33F/73F and MX25L12872F if you need to use the SPB features.

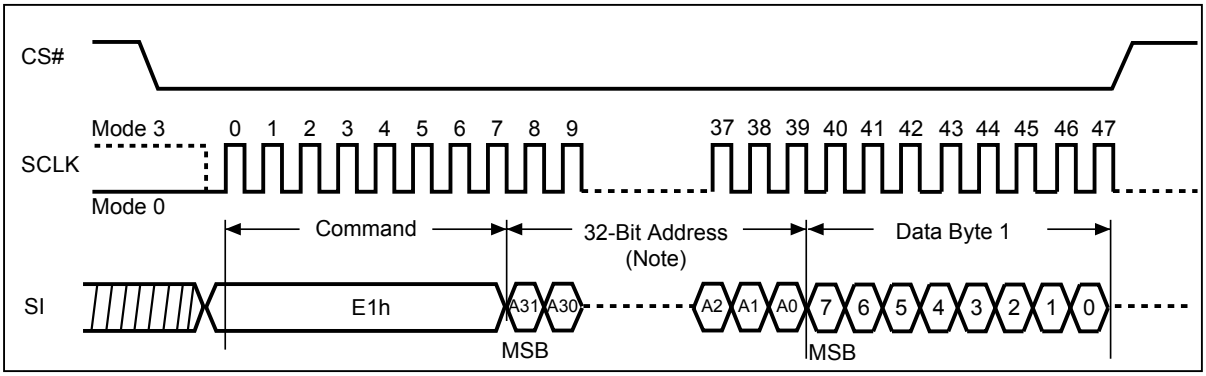
The SPB protection can also temporary unprotect by solid write protect bit (USPB) feature (only provided by MX25L12835F/73F) to temporarily unprotect the sectors protected by SPB.

To modify the DPB status, issue the DPB Program command (WRDPB) including the target sector or block address and set or clear the DPB protection state. All DPB bits can be quickly unlocked by issuing one Gang Block Unlock (GBULK) command (98h). Sector selection is made using address bits A23-A12 and only the top and bottom sixteen 4KB sectors can be individually protected. The remaining sectors are grouped into 64KB blocks. Individual 64KB block selection is made using address bits A23-A16.

Table 2-4: DPB Register

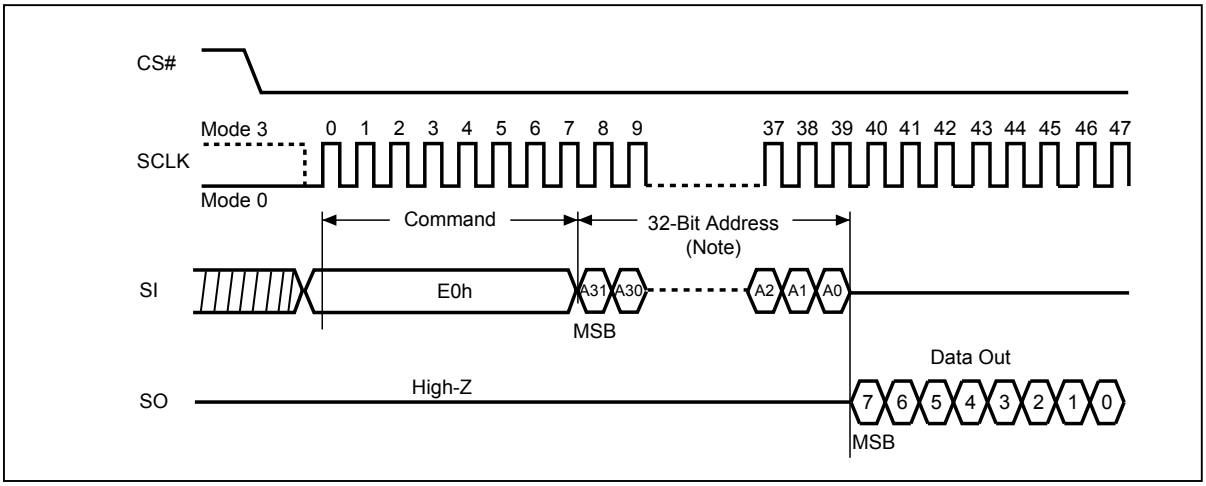
Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic Protection Bit)	00h= Unprotect Sector / Block FFh= Protect Sector / Block	FFh	Volatile

Figure 2-1: Write DPB Register (WRDPB) Sequence



Note: *A31-A24 are don't care.*

Figure 2-2: Read DPB Register (RDDPB) Sequence



Note: *A31-A24 are don't care.*

2-2-4 Lock Register

Operating individual sector protection feature on MX25L12835F/33F/73F and MX25L12872F is similar. All of them have SPB and DPB to implement individual sector protection feature.

To enhance the security of the protection feature, both MX25L12833F and MX25L12872F provide SPB Lock Down feature, once SPBLKDN (bit 6) is set, SPB bit value cannot be changed again and it is read-only.

The Lock Register has slight difference. Please refer to the comparison table (*Table 2-5: Lock Register Comparison*) and refer to MX25L12835F/33F/73F and MX25L12872F datasheets for more detailed information.

Table 2-5: Lock Register Comparison

	MX25L12835F MX25L12873F	MX25L12833F MX25L12872F
bit 0	Reserved	Reserved
bit 1	Solid Protection Mode Lock Bit	Reserved
bit 2	Password Protection Mode Lock Bit	Reserved
bit 3	Reserved	Reserved
bit 4	Reserved	Reserved
bit 5	Reserved	Reserved
bit 6	Reserved	SPBLKDN
bit 7-15	Reserved	Reserved

3. Performance Comparison

Please note that the maximum frequency can only be supported under 3.0V-3.6V of Quad I/O for both MX25L12833F and MX25L12872F.

Table 3-1: Read Performance Comparison

Read Performance	MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
VCC	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V	2.7V-3.6V
Normal Read (1-1-1)	50MHz	50MHz	50MHz	50MHz
FASTREAD (1-1-1)	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**
DREAD (1-1-2)	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**
2READ (1-2-2)	84MHz* 133MHz**	84MHz* 133MHz**	84MHz* 133MHz**	84MHz* 133MHz**
QREAD (1-1-4)	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**	104MHz* 133MHz**
4READ (1-4-4)	84MHz* 133MHz**	84MHz* 133RMHz**	84MHz* 133MHz**	84MHz* 133RMHz**
QPI (4-4-4)	84MHz* 133MHz**	84MHz* 133RMHz**	84MHz* 133MHz**	84MHz* 133MHz**
Configurable Dummy Cycles	Yes	Yes	Yes	Yes

Notes: 1. * means default status. ** means Maximum Value.
2. R means VCC range = 3.0V-3.6V.

Table 3-2: AC Performance Comparison

AC Performance		Condition	MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
Erase Time	4KB	typ	30ms	25ms	30ms	25ms
		max.	120ms	120ms	120ms	120ms
	32KB	typ.	0.15s	0.14s	0.15s	0.14s
		max.	0.65s	0.65s	0.65s	0.65s
	64KB	typ.	0.28s	0.25s	0.28s	0.25s
		max.	0.65s	0.65s	0.65s	0.65s
	Chip Erase	typ.	50s	26s	50s	26s
		max.	80s	60s	80s	60s
Program Time	256Byte	typ.	0.5ms	0.33ms	0.5ms	0.33ms
		max.	1.5ms	1.2ms	1.5ms	1.2ms
Clock Low to Output Valid	15pf	max.	6ns	6ns	6ns	6ns
	30pf	max.	8ns	8ns	8ns	8ns

Table 3-3: DC Performance Comparison

DC Performance		MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
Active Current (max.)	Read (4I/O)	25mA	25mA	25mA	25mA
	Erase	25mA	25mA	25mA	25mA
	Program	20mA	20mA	20mA	20mA
VCC Standby Current		10uA(typ.)/ 50uA(max.)	10uA(typ.)/ 50uA(max.)	10uA(typ.)/ 50uA(max.)	10uA(typ.)/ 50uA(max.)
Deep Power Down Current		2uA(typ.)/ 20uA(max.)	2uA(typ.)/ 20uA(max.)	2uA(typ.)/ 20uA(max.)	2uA(typ.)/ 20uA(max.)

Note: *All of the data shown in the table are maximum values unless noted as typical.*

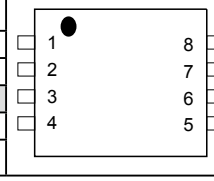
4. Package and Pinout Comparison

Figure 4-1 shows the common packages and the pinout assignments for the devices. The MX25L12873F and MX25L12872F do not support WP# and Hardware RESET# function.

Figure 4-1: Packages and Pinouts

8-PIN SOP (200mil)

MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
CS#	CS#	CS#	CS#
SO/SIO1	SO/SIO1	SO/SIO1	SO/SIO1
WP#/SIO2	WP#/SIO2	SIO2	SIO2
GND	GND	GND	GND



MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
VCC	VCC	VCC	VCC
RESET#/SIO3	RESET#/SIO3	SIO3	SIO3
SCLK	SCLK	SCLK	SCLK
SI/SIO0	SI/SIO0	SI/SIO0	SI/SIO0

5. Command Code Comparison

All of the commands are listed in **Table 5-1** below. Most commands are common. Differences are attributted to unsupported or new features.

Table 5-1: Command Code Comparison (ID Read/Read/Erase/Program/Mode)

Command	Symbol	Description	MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
ID Read	RDID	Read Identification	9Fh	9Fh	9Fh	9Fh
	RES	Read Electronic ID	ABh	ABh	ABh	ABh
	REMS	Read Electronic Manufacturer & Device ID	90h	90h	90h	90h
	REMS2	2 x I/O Read ID	-	-	-	-
	REMS4	4 x I/O Read ID	-	-	-	-
	QPIID	QPI ID Read	AFh	AFh	AFh	AFh
Read	READ	Read Data	03h	03h	03h	03h
	FAST READ	Fast Read	0Bh	0Bh	0Bh	0Bh
	2READ	2 x I/O Fast Read	BBh	BBh	BBh	BBh
	DREAD	1I 2O Fast Read	3Bh	3Bh	3Bh	3Bh
	4READ	4 x I/O Fast Read	EBh	EBh	EBh	EBh
	QREAD	1I 4O Fast Read	6Bh	6Bh	6Bh	6Bh
	W4READ	4 x I/O Fast Read with 4 dummy clock cycles	-	-	-	-
	FASTDTRD	Fast DT Read	-	-	-	-
	2DTRD	Dual I/O DT Read	-	-	-	-
	4DTRD	Quad I/O DT Read	-	-	-	-
	RDSFDP	-	5Ah	5Ah	5Ah	5Ah
Erase	SE	Sector Erase	20h	20h	20h	20h
	BE (64K)	Block Erase 64KB	D8h	D8h	D8h	D8h
	BE (32K)	Block Erase 32KB	52h	52h	52h	52h
	CE	Chip Erase	60h or C7h	60h or C7h	60h or C7h	60h or C7h
Program	PP	Page Program	02h	02h	02h	02h
	4PP	Quad Page Program	38h	38h	38h	38h
	CP	Continuously Program Mode	-	-	-	-
Mode	WREN	Write Enable	06h	06h	06h	06h
	WRDI	Write Disable	04h	04h	04h	04h
	DP	Deep Power Down	B9h	B9h	B9h	B9h
	RDP	Release from Deep Power Down	ABh	ABh	ABh	ABh
	EQIO	Enable QPI	35h	35h	35h	35h
	RSTQIO	Reset (Exit) QPI	F5h	F5h	F5h	F5h
	SBL	Set Burst Length	C0h	C0h	C0h	C0h
	WPSEL	Write Protect Selection	68h	68h	68h	68h
	ESRY	Enable SO to Output RY/BY#	-	-	-	-
	DSRY	Disable SO to Output RY/BY#	-	-	-	-
	ENPLM	Enter Parallel Mode	-	-	-	-
	EXPLM	Exit Parallel Mode	-	-	-	-
	HPM	High Performance Mode Enable	-	-	-	-
	ENSO	Enter Secured OTP	B1h	B1h	B1h	B1h
	EXSO	Exit Secured OTP	C1h	C1h	C1h	C1h
	PGM/ERS Suspend	Suspend Program/ Erase	B0h	75h or B0h	B0h	75h or B0h
	PGM/ERS Resume	Resume Program/ Erase	30h	7Ah or 30h	30h	7Ah or 30h

Table 5-1: Command Code Comparison (Reset/Register/Protection)

Command	Symbol	Description	MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
Reset	NOP	No Operation	00h	00h	00h	00h
	RSTEN	Reset Enable	66h	66h	66h	66h
	RST	Reset Memory	99h	99h	99h	99h
	CLSR	Clear SR Fail Flags	-	-	-	-
Register	WRSR	Write Status Register	01h	01h	01h	01h
	RDSR	Read Status Register	05h	05h	05h	05h
	RDSCUR	Read Security Register	2Bh	2Bh	2Bh	2Bh
	WRSCUR	Write Security Register	2Fh	2Fh	2Fh	2Fh
	RDCR	Read Configuration Register	15h	15h	15h	15h
	RDFBR	Read Fast Boot Register	16h	-	16h	-
	WRFBR	Write Fast Boot Register	17h	-	17h	-
	ESFBR	Erase Fast Boot Register	18h	-	18h	-
Protection	SBLK	Single Block Lock	-	-	-	-
	SBULK	Single Block Unlock	-	-	-	-
	RDBLOCK	Block Protect Read	-	-	-	-
	GBLK	Gang Block Lock	7Eh	7Eh	7Eh	7Eh
	GBULK	Gang Block Unlock	98h	98h	98h	98h
	WRLR	Write Lock Register	2Ch	2Ch	2Ch	2Ch
	RDLR	Read Lock Register	2Dh	2Dh	2Dh	2Dh
	RDPASS	Read Password Register	27h	-	27h	-
	WRPASS	Write Password Register	28h	-	28h	-
	PASSULK	Password Unlock	29h	-	29h	-
	RDSPB	Read SPB Status	E2h	E2h	E2h	E2h
	WRSPB	SPB bit Program	E3h	E3h	E3h	E3h
	ESSPB	All SPB bit Erase	E4h	E4h	E4h	E4h
	SPBLK	SPB Lock Set	A6h	-	A6h	-
	RDSPBLK	Read SPB Lock Register	A7h	-	A7h	-
	RDDPB	Read DPB Register	E0h	E0h	E0h	E0h
	WRDPB	Write DPB Register	E1h	E1h	E1h	E1h

6. Device ID Code Comparison

The Manufacturer and Device IDs are not changed, as shown in **Table 6-1**.

Table 6-1: ID Code Comparison

Electronic Identification		MX25L12835F	MX25L12833F	MX25L12873F	MX25L12872F
RDID	Manufacturer ID	C2h	C2h	C2h	C2h
	Type	20h	20h	20h	20h
	Density	18h	18h	18h	18h
RES	Electronic ID	17h	17h	17h	17h
REMS/REMS2/ REMS4	Manufacturer ID	C2h	C2h	C2h	C2h
	Device ID	17h	17h	17h	17h

7. Summary

The MX25L12872F is backward compatible with most of the common commands and features of MX25L12835F/33F/73F.

The MX25L12833F and MX25L12872F have additional 8K-bit secured OTP mode, while MX25L12835F/73F have additional 4K-bit secured OTP mode. Furthermore, MX25L12833F and MX25L12872F do not provide fast boot mode and password protection.

The Quad I/O mode is permanently enabled on MX25L12873F and MX25L12872F.

8. References

Table 8-1 shows the datasheet versions used for comparison in this application note. For the most current Macronix specification, please refer to the Macronix Website at *http://www.macronix.com*

Table 8-1: Datasheet Version

Datasheet	Location	Date Issued	Versions
MX25L12835F	Macronix Website	July 22, 2016	1.6
MX25L12833F	Macronix Website	October 17, 2017	1.0
MX25L12873F	Macronix Website	July 22, 2016	1.2
MX25L12872F	Macronix Website	October 17, 2017	1.0

9. Revision History

Table 9-1: Revision History

Revision No.	Description	Page	Date
Rev. 1	Initial Release	ALL	September 08, 2017
Rev. 2	Updated MX25L12833F and MX25L12872F Program and Erase values	7, 10	October 17, 2017
Rev. 3	Updated datasheet issued date	10	October 19, 2017
Rev. 4	Added feature information of permanently enabled 4 I/O mode	1, 2	November 09, 2017
Rev. 5	1. Revised the Active Current of Read (4I/O) and Program 2. Added "Macronix Proprietary" footnote	7, ALL	July 10, 2018
Rev. 6	1. Added 6x5mm 8-WSON for MX25L12872F in Comparison table.	2	August 27, 2019

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