Plastic Package Device Thermal Resistance

Introduction

This document discusses the thermal characteristics of Macronix plastic packaged devices in order to help system designers avoid exceeding the maximum temperature specification of a flash memory device.

Terms and definitions

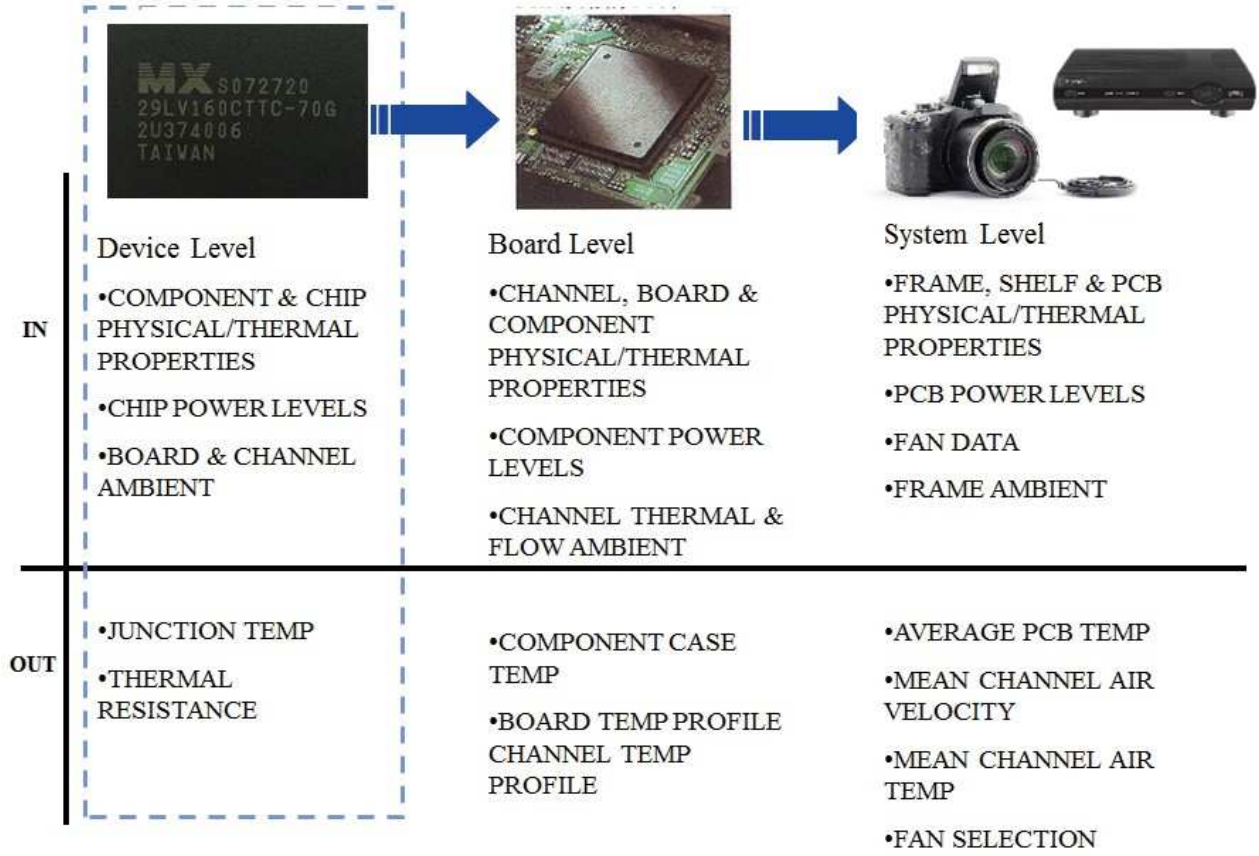
[ref1]

- T_J: Die Junction Temperature (°C)
- T_A: Ambient Temperature or Local Environment Temperature (°C)
- T_C: Case Temperature or Top Center of Package Surface Temperature (°C)
- P_D: Power Dissipation (W)
- Θ_{JA}: Junction-to-Ambient Thermal Resistance (°C/W)
- Θ_{JC}: Junction-to-Case Thermal Resistance (°C/W)

Background

Thermal system design needs to account for heat transfer at many levels: device, board, and system level (*"Figure 1. Thermal Factors at Different System Levels"*). In this document we focus on device level thermal resistance, the relationship between T_J and T_C, and how heat is dispersed through the air and board.

Figure 1. Thermal Factors at Different System Levels



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Thermal Resistance and Heat Transfer

Good thermal system design is critical to ensure proper system performance, reliability, and lifetime.

As shown in *"Figure 1. Thermal Factors at Different System Levels"* above, PCB design (layer, pad size.) and air flow are major factors affecting heat dissipation. At the component level, many factors can affect thermal resistance such as package type, package material, chip size, power dissipation, etc.

"Figure 2. Forms of Heat Transfer." shows a schematic of heat dissipation paths at the device level. The primary mechanisms for heat transfer at the component level are Convection (heat transfer from the surface of the package to the ambient typically through air flow) and Conduction (heat transfer from the die surface through bond wires and lead frame to PC board). Heat transfer by Radiation (electromagnetic energy transfer) is typically negligible for flash memory devices. In the plastic packages used by Macronix for flash memory, generally 5~20% of the heat dissipated is through the top of the package via convection while the remaining 80~95% is through the PCB via conduction. *"Figure 3. a). Thermal Resistance vs Laminar Air Flow"*, *"Figure 3. b). Thermal Resistance vs Chip Size"*, and *"Figure 3. c). Thermal Resistance vs PCB Design"* show the effects of various factors on thermal resistance.

Figure 2. Forms of Heat Transfer.

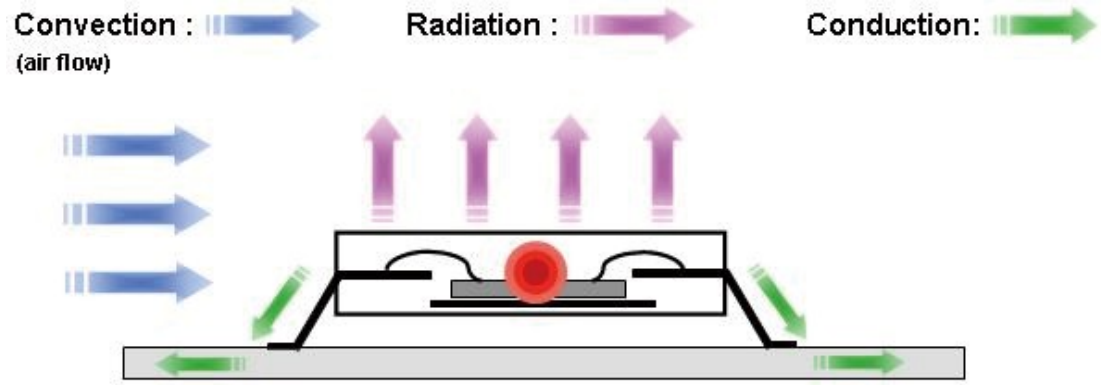

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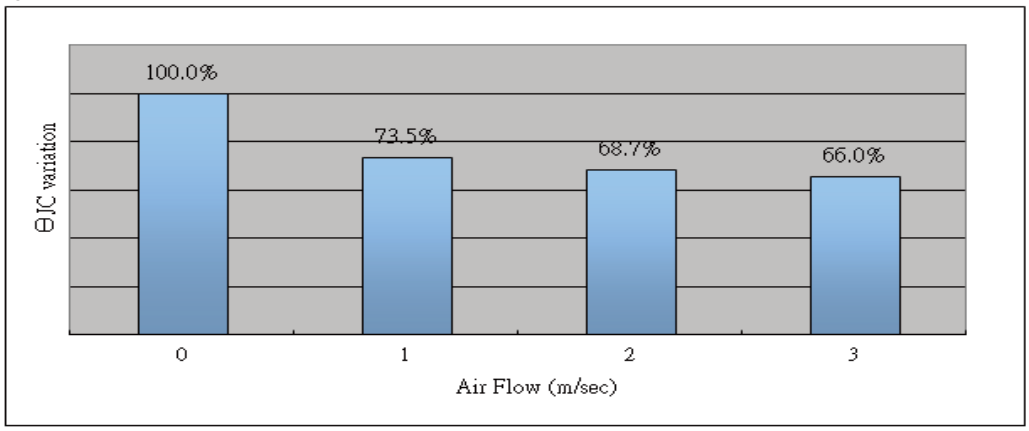
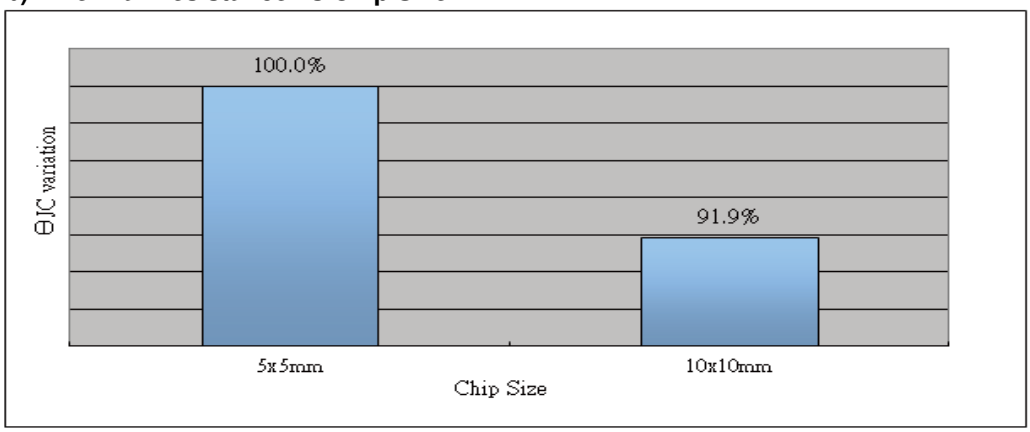
Figure 3. a). Thermal Resistance vs Laminar Air Flow



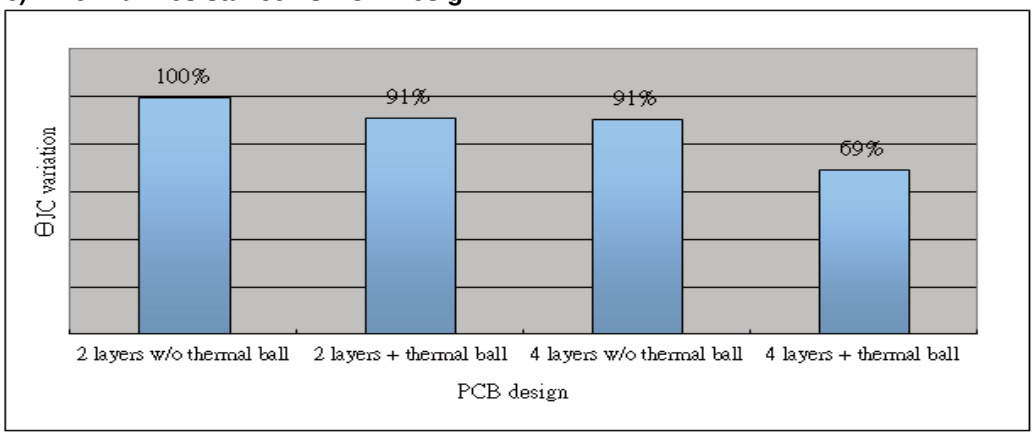
Note: 14x20mm 56 TSOP package with a power dissipation of 0.36W

Figure 3. b). Thermal Resistance vs Chip Size



Note: 14x20mm 56 TSOP package with a power dissipation of 0.36W.

Figure 3. c). Thermal Resistance vs PCB Design



Note: 352ball PBGA with a power dissipation of 1.5W.

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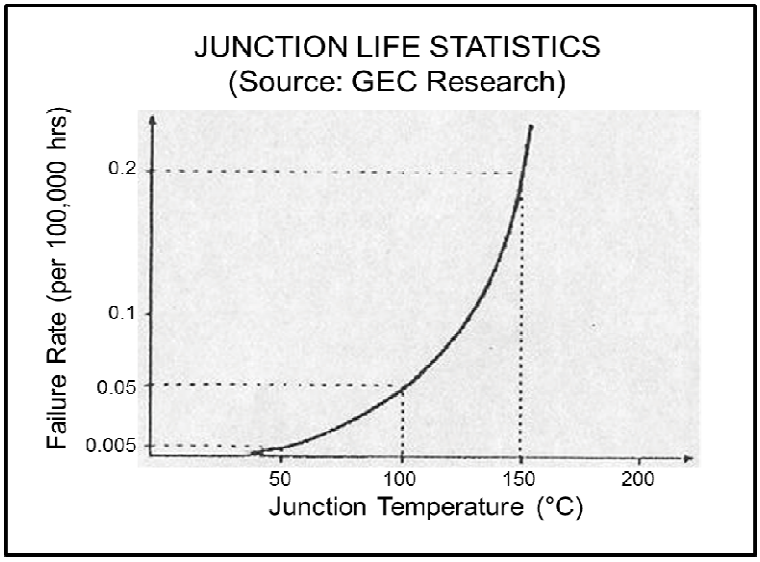
In general, flash performance and lifetime is reduced as die junction temperature is increased (*"Figure 4. Relationship between Device Lifetime and Die Junction Temperature."*).

Figure 4. Relationship between Device Lifetime and Die Junction Temperature.



Source from GEC Research

Therefore, it is best to keep die junction temperatures at the low end of datasheet limits as much as possible. The die Junction temperature (Tj) can be calculated by adding the Self Heating of the die (due to internal power dissipation during device operation) to the ambient temperature (Ta) surrounding the flash in the system.

Tj = Self Heating + Ta (where: Self Heating=(Θ_{JA} * P), P=V * I) [eq 1]
After expanding the equation:
Tj = (Θ_{JA} * V * I) + Ta

From *equation 1*, we can see that in order to reduce the die junction temperature, we should try to reduce the system ambient temperature and/or reduce the flash self-heating.

To reduce the ambient temperature and reduce the case-to-ambient thermal resistance, we can improve air flow with additional ventilation, the addition of fans, or the introduction of other types of system cooling mechanisms, for example, water, fins, etc. These solutions may not be practical due to increased system cost and size. We can also move the flash memory away from other heat producing chips such as high powered controllers. Unfortunately this may not be practical due to signal integrity issues where it is beneficial to have the flash memory as close to the controller as possible for high speed operation.

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The self-heating of flash memory die can be reduced by reducing the operating voltage and/or clock frequency. However, this may lead to a negative impact on the system performance. Even the reduction of clock frequency may only have a minimal effect, as both the Program and Erase functions in many flash memories are executed with internal self-timed algorithms, independent of clock frequency.

Lastly, let's discuss Θ_{JC}, which is the thermal resistance of the package containing the flash.

Θ_{JC} Derivation

From Fourier's Law for thermal conduction:
$P = -kA(dT/dx)$ *[ref2]*
Where:
dT/dx = temperature gradient (°C/m)
k = material thermal conductivity (W/m °C) P=Heat
Flow (W) normal to transfer area A ($m^{\wedge 2}$)

$$P = -kA(dT/dx)$$
$$\int dT = \int (P/kA)\, dx$$
$$\Delta T = (L/kA) * P \quad \text{[eq 2]}$$
$$\Delta T = \Theta * P$$
$$Tjc = (\Theta_{JC}) * P \quad \text{(where: } \Theta_{JC} \text{ is Thermal Resistance (°C/W) from junction to case)}$$
or:
$$\Theta_{JC} = (T_J - T_C) / P_D \quad \text{[eq 3]}$$

Θ_{JC} can be calculated and used to assess ability of heat spreading out through top or bottom of package.

From a package level viewpoint:

From *equation 2* above, we can see that in order to reduce the package thermal resistance (Θ_{JC}) we can either reduce the thickness (L) of the package material, increase the cross section area of the die (A), or select a more thermally conductive plastic mold compound (k). Adding thermal vias, a heat slug in the package, or even more device pins can help reduce the package thermal resistance by providing a lower thermal resistance path from the die surface through the package. Package type, material, device size, and PCB design all have some effect on the die junction temperature. For example, with the same level of power dissipation, the same chip with a different package type (ex: TSOP vs. PDIP) may produce a different die junction temperature.

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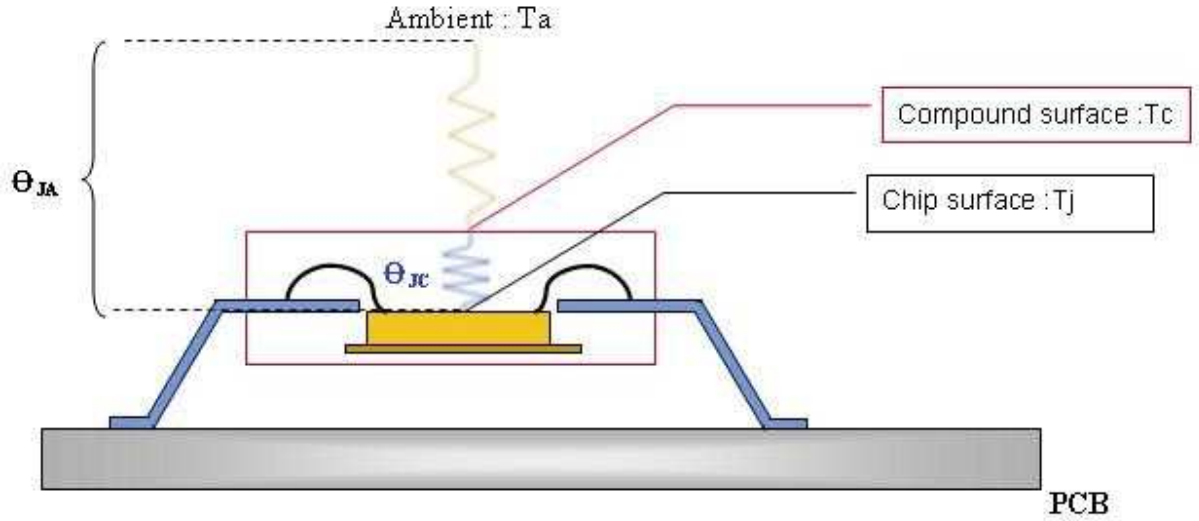
Thermal Resistance Measurement and Application

"Figure 5. Diagram of Thermal Resistance Relationships (ΘJC & ΘJA)." shows the relationship between the thermal resistances, the die junction, the package case, and the surrounding ambient temperature.

Figure 5. Diagram of Thermal Resistance Relationships (Θ_{JC} & Θ_{JA}).



If we measure Tj and Ta with a thermal couple in a standard test environment, Θ_{JA} can be calculated per *equation 4*, where P_D = Power Dissipation in test.

$$\Theta_{JA} = (Tj - Ta) / P_D \qquad \text{[eq 4]}$$

A lower Θ_{JA} means that the heat generated by the chip while in operation is more easily removed through the top of the package into the surrounding ambient air and through the leads to the PC board. If two different packages have the same Θ_{JA}, it means they have equal thermal performance in the same operating environment.

If Θ_{JA} in a given application is known, the die junction temperature can be calculated for any ambient temperature using the same equation.

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Thermal Temperature Specification

Macronix flash memory device power dissipation, under normal conditions, is relatively small and therefore the resulting die junction temperatures are typically well below junction breakdown temperatures that can cause reliability concerns. Please refer to JEDEC standard JESD51 for the measurement methodology used to generate the thermal temperature data in *"Table-2: Die Junction to Ambient and Junction to Case Typical Thermal Resistance (Θ_{JA} & Θ_{JC})"*. For more accurate or special requirements, Finite Element Analysis (FEA) should be used.

Table-1 Ambient, Die Junction, and Device Storage Maximum Temperature Range

Package Type	Application	Ambient Operating Temperature (Ta , °C)	Die Junction Functional Temperature Range[1] (TJ , °C)	Storage Temperature Range (°C)
All	Commercial	0 ~ 70	-40 ~ 125[1]	-60 ~ 150
	Industrial	-40 ~ 85	-40 ~ 125[1]	-60 ~ 150
	Automotive S Grade	-40 ~ 85	-40 ~ 125[1]	-60 ~ 150
	Automotive R Grade	-40 ~ 105	-40 ~ 125[1]	-60 ~ 150
	Automotive Q Grade	-40 ~ 125	-40 ~ 130[1&3]	-60 ~ 150

Table-2 Die Junction to Ambient and Junction to Case Typical Thermal Resistance (Θ_{JA} & Θ_{JC})

Package type	Lead/Ball	Package size	Thermal Resistance[2] (ΘJA , °C/W)	Thermal Resistance[2] (ΘJC , °C/W)
PDIP	8	300mil	67.5	36.7
SOP	8	150mil	116.6	44.0
SOP	8	209mil	77.5	45.2
SOP	16	300mil	84.9	20.6
VSOP	8	150mil	111.23	24.02
VSOP	8	209mil	93.8	20.62
USON	8	2x3mm	84.8	30.4
USON	8	4x3mm	87.8	40.1
USON	8	4x4mm	41.4	14.3
WSON	8	6x5mm	39.2	29.1
WSON	8	8x6mm	44.8	14.6
TSOP	48	Type-I	90.0	16.0
TSOP	56	Type-I	64.4	9.4
BGA	24	6x8mm	65.7	19.2
BGA	48	6x8mm	57.3	19.2
BGA	56	7x9mm	29.4	7.3
BGA	63	9x11mm	24.2	3.9
BGA	64	11x13mm	57.3	17.6
BGA	130	8x9mm	32.3	6.1
BGA	153	11.5x13mm	45.04	3.42
BGA	153	11x10mm	47.74	3.05
BGA	162	8x10.5mm	30.4	4.1

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**Note-1: The temperature range provided in "Table-1 Die Junction Functional Range (TJ, °C)" are absolute maximum stress rating. Stress over the range may cause permanent damage on flash. For the die junction and case temperature to meet datasheet specification operating, please refer to the next section of "Example Die Junction and Case Temperature Calculation".*

**Note-2: Thermal Resistance values provided in "Table-2 Die Junction to Ambient and Junction to Case Typical Thermal Resistance (ΘJA & ΘJC)" are typical values obtained while device operates within datasheet voltage/current power limits in still air (air flow = 0m/sec). Implementing a heat dissipating design (ex: additional air flow / heat sink / PCB layers, etc.) is recommend in high temperature applications.*

**Note-3: For Automotive Q grade products, if the calculated Tj(max) exceeded the value stated here, Macronix needs to perform additional qualification tests on specified product which may incur Non-Recurring Engineer (NRE) expense for ensuring the product functionality.*

Example Die Junction and Case Temperature Calculation

In this example we will calculate the maximum die junction temperature and case temperature seen by an MX25L8006EM1I-12G, which is an Industrial grade, 3V, Macronix Serial NOR Flash memory in a 150mil 8SOP package.

The MX25L8006EM1I-12G has the following thermal resistances: Θ_{JA} = 116.6°C/W and Θ_{JC} = 44°C/W

The thermal resistance numbers in our example are for our example calculation purposes only. Please contact your Macronix Sales if thermal resistance numbers are needed for the Macronix package and die density you are using because the thermal resistance values may be different.

According to the MX25L8006EM1I-12G datasheet:
Max Power Dissipation (P_D) = V * I = 3.6V * 20mA = 72mW Max
Ambient Temperature (Ta) = 85°C
Tj = Ta + (PD * Θ_{JA}) = 85°C + (72mW * 116.6°C/W) = 85°C + 8.4°C = 93.4°C
Tc = Tj – (PD * Θ_{JC}) = 93.4°C – (72mW * 44°C/W) = 93.4°C – 3.2°C = 90.2°C

References

[1] JESD88E "JEDEC Dictionary of Terms for Solid-State Technology — 6th Edition" June 2013

[2] R. R. Tummala and E.J. Rymaszewski. Microelectronics Packaging Handbook" Copyright 1989 Van Norstrand Reinholdt. P171.

EIAJ/JEDEC EIA/JESD51-1: INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD-ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE)

EIAJ/JEDEC EIA/JESD51-2: INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIROMENTAL CONDITIONS-NATURAL CONVENCTION (STILL AIR)

SEMI G42-96: SPECIFICATION FOR THERMAL TEST BOARD STANDARIZATION FOR MEASURING JUNCTION-TO-AMBIENT THERMAL RESISTANCE OF SEMICONDUCTOR PACKAGES

SEMI G38-96: TEST METHOD FOR STILL- AND FORCE-AIR JUNCTION-TO-AMBIENT THERMAL RESISTANCE MEASUREMENTS OF INTEGRATED CIRCUIT PACKAGES.

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Revision History

Revision No.	Date	Description
REV. 1	Nov. 2013	Initial Release.
REV. 2	May 2014	Allocate *"Table-1 Ambient, Die Junction, and Device Storage Maximum Temperature Range"* to page-7. Add *"Table-2 Die Junction to Ambient and Junction to Case Typical Thermal Resistance (ΘJA & ΘJC)"* with thermal resistance number.
REV. 3	Jun. 2014	Add the 48-BGA data.
REV. 4	Jul. 2015	Modified "Example Die Junction and Case Temperature Calculation" Add the 8-USON (4x3mm), 8-VSOP (150mil & 209mil), 130-BGA and 162-BGA data.
REV. 5	Apr. 2016	Add note for "Die Junction Functional Range"
REV. 6	Mar. 2017	Remove ΘCA to follow JEDEC/JESD51 definition.
REV. 7	Nov. 2017	Add the 153-BGA data.
REV. 8	Jul. 2020	Add the 153-BGA (11x10mm) data.
REV. 9	Dec. 2020	Add Automotive Q Grade data.

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For the contact and order information, please visit Macronix's Web site at: http://www.macronix.com