MX66U2G45G - J Grade

1.8V, 2G-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Support DTR (Double Transfer Rate) Mode*
- *8/16/32/64 byte Wrap-Around Read Mode*

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1.8V 2G-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 1.7 to 2.0 volt for read, erase, and program operations
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Fast read for SPI mode
  - Support fast clock frequency up to 166MHz
  - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Support DTR (Double Transfer Rate) Mode
  - Configurable dummy cycle number for fast read operation
- Support Performance Enhance Mode - XIP (execute-in-place)
- Quad Peripheral Interface (QPI) available
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
  - Advanced sector protection function
- Additional 8K bit security OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O read mode and 4 x I/O read mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O read mode
- NC/SIO3
  - No Connection or Serial input & Output for 4 x I/O read mode
- RESET#
  - Hardware Reset pin
- PACKAGE
  - 24-Ball BGA (5x5 ball array)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX66U2G45G is 2Gb bits Serial NOR Flash memory, which is configured as 268,435,456 x 8 internally. When it is in two or four I/O mode, the structure becomes 1,073,741,824 bits x 2 or 536,870,912 bits x 4. MX66U2G45G features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI, SO, WP# and NC pins become SIO0, SIO1, SIO2 and SIO3 pins for address/dummy bits input and data output.

The MX66U2G45G MXSMIO® (Serial Multi I/O) provides sequential read operation on the whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Erase command is executed on 4K-byte sector, 32K-byte block, or 64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

Advanced security features enhance the protection and security functions, please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode.

The MX66U2G45G utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

Table 1. Read performance Comparison

Numbers of Dummy Cycles	Fast Read (MHz)	Dual Output Fast Read (MHz)	Quad Output Fast Read (MHz)	Dual IO Fast Read (MHz)	Quad IO Fast Read (MHz)	Quad I/O DT Read (MHz)
4	-	-	-	84*	70	42
6	133	133	104	104	84*	52*
8	133*	133*	133*	133	104	66
10	166	166	166	166	133	102

Note: * mean default status

3. PIN CONFIGURATIONS

24-Ball BGA (5x5 ball array)

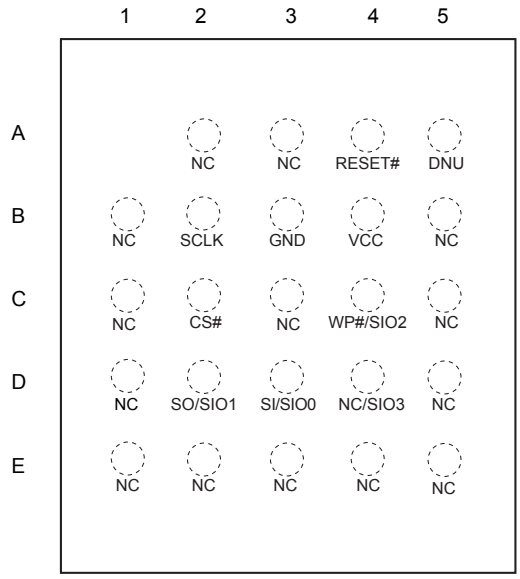


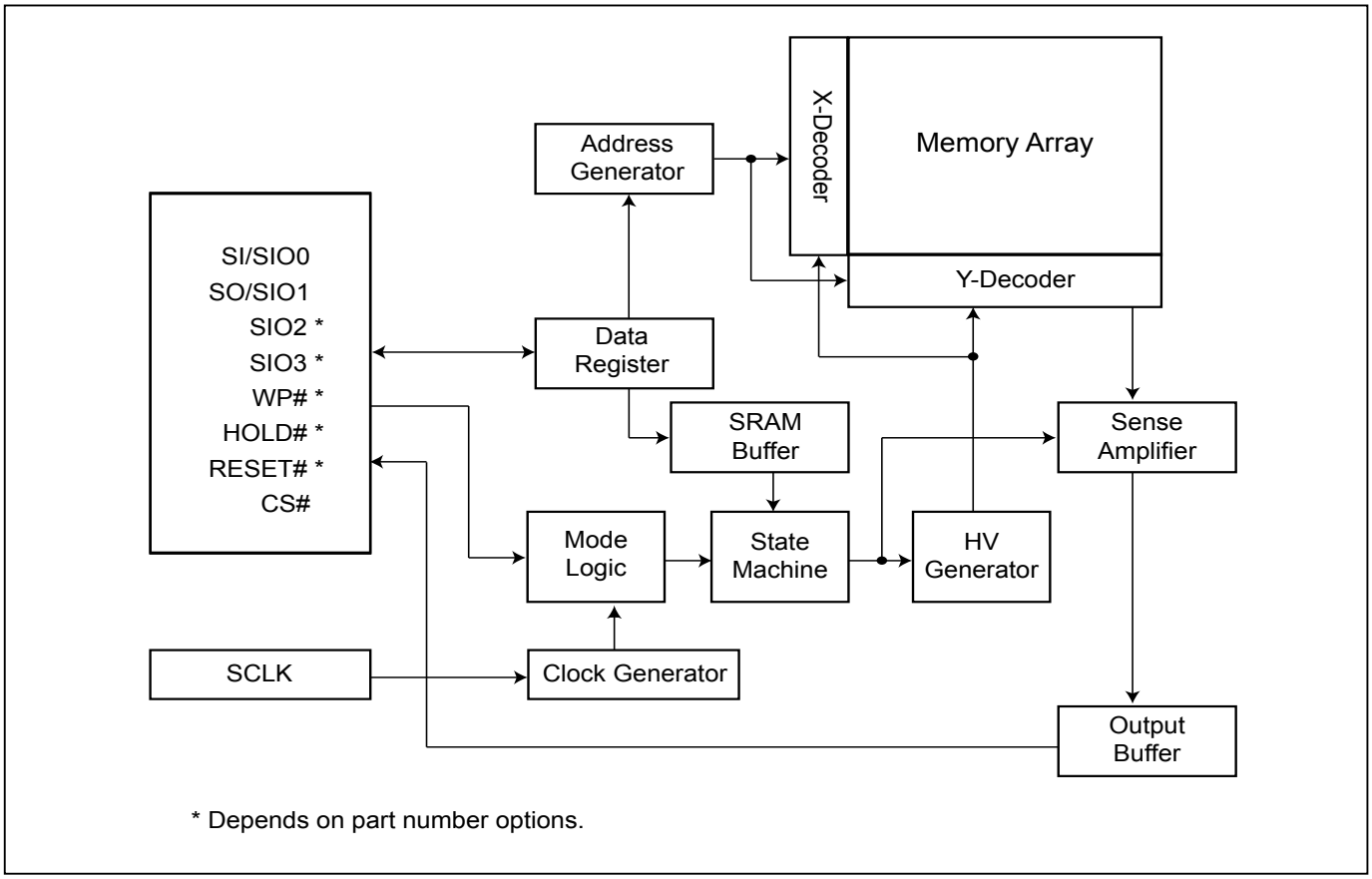
Table 2. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SCLK	Clock Input
RESET#	Hardware Reset Pin Active low (Note1)
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O read mode)
WP#/SIO2	Write Protection Active Low or Serial Data Input & Output (for 4xI/O read mode)
NC/SIO3	No Connection or Serial Data Input & Output (for 4xI/O read mode)
VCC	Power Supply
GND	Ground
NC	No Connection
DNU	Do Not Use (It may connect to internal signal inside)

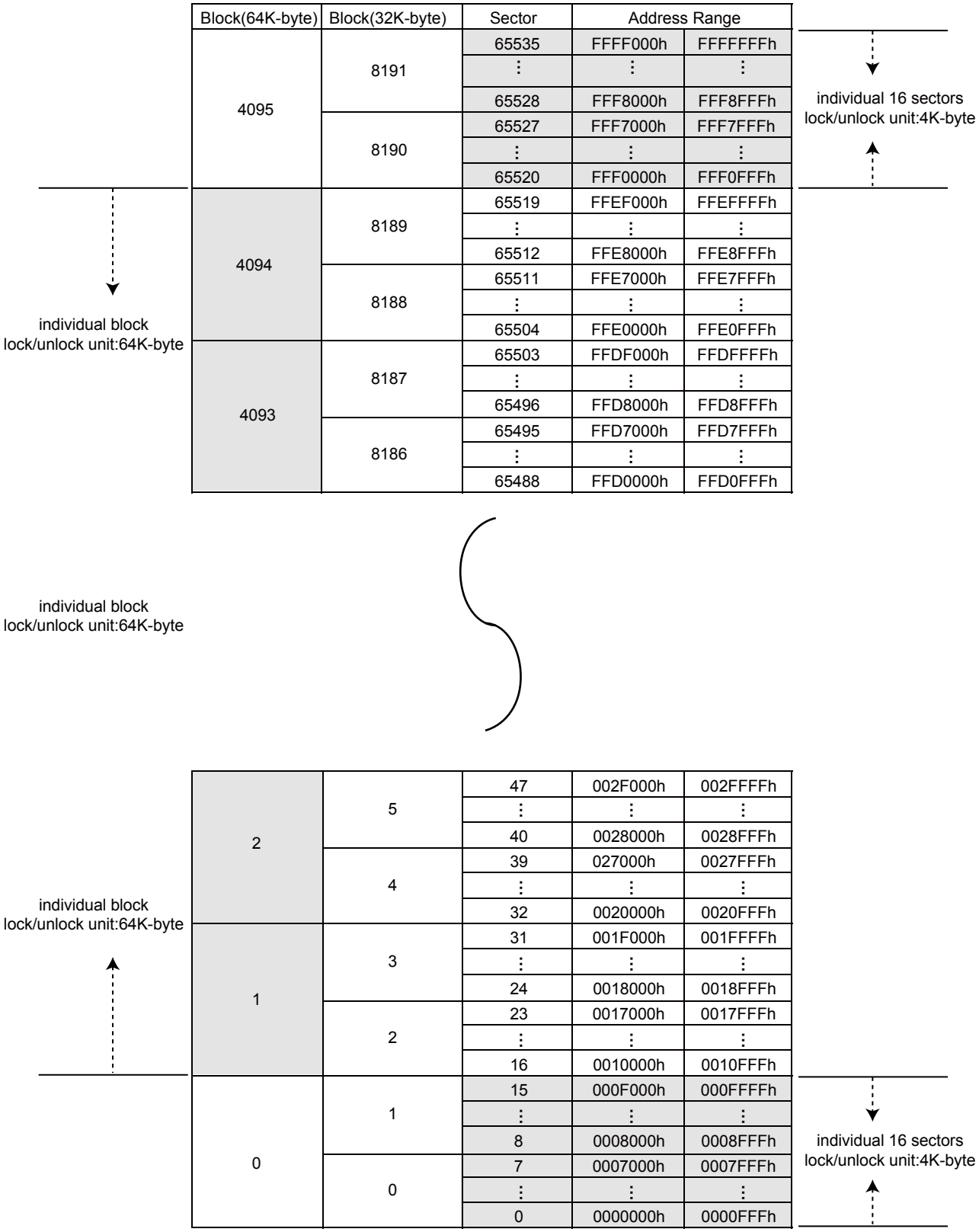
Note:

1. The pin of RESET# or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration.
   However, the internal pull up function will be disabled if the system has physical connection to RESET# or WP#/SIO2 pin.

4. BLOCK DIAGRAM



5. MEMORY ORGANIZATION



Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
4095	8191	65535	FFFF000h	FFFFFFFh
		⋮	⋮	⋮
		65528	FFF8000h	FFF8FFFh
	8190	65527	FFF7000h	FFF7FFFh
		⋮	⋮	⋮
		65520	FFF0000h	FFF0FFFh
4094	8189	65519	FFEF000h	FFEFFFFh
		⋮	⋮	⋮
		65512	FFE8000h	FFE8FFFh
	8188	65511	FFE7000h	FFE7FFFh
		⋮	⋮	⋮
		65504	FFE0000h	FFE0FFFh
4093	8187	65503	FFDF000h	FFDFFFFh
		⋮	⋮	⋮
		65496	FFD8000h	FFD8FFFh
	8186	65495	FFD7000h	FFD7FFFh
		⋮	⋮	⋮
		65488	FFD0000h	FFD0FFFh
2	5	47	002F000h	002FFFFh
		⋮	⋮	⋮
		40	0028000h	0028FFFh
	4	39	027000h	0027FFFh
		⋮	⋮	⋮
		32	0020000h	0020FFFh
1	3	31	001F000h	001FFFFh
		⋮	⋮	⋮
		24	0018000h	0018FFFh
	2	23	0017000h	0017FFFh
		⋮	⋮	⋮
		16	0010000h	0010FFFh
0	1	15	000F000h	000FFFFh
		⋮	⋮	⋮
		8	0008000h	0008FFFh
	0	7	0007000h	0007FFFh
		⋮	⋮	⋮
		0	0000000h	0000FFFh

6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), Erase/Program suspend command, Erase/Program resume command and softreset command.
- Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

6-1. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 3. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.
- The Hardware Protected Mode (HPM) use WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and Status Register Write Protect bit.
- In four I/O and QPI mode, the feature of HPM will be disabled.

Table 3. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	2Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 4095th)
0	0	1	0	2 (2 blocks, protected block 4094th-4095th)
0	0	1	1	3 (4 blocks, protected block 4092nd-4095th)
0	1	0	0	4 (8 blocks, protected block 4088th-4095th)
0	1	0	1	5 (16 blocks, protected block 4080th-4095th)
0	1	1	0	6 (32 blocks, protected block 4064th-4095th)
0	1	1	1	7 (64 blocks, protected block 4032nd-4095th)
1	0	0	0	8 (128 blocks, protected block 3968th-4095th)
1	0	0	1	9 (256 blocks, protected block 3840th-4095th)
1	0	1	0	10 (512 blocks, protected block 3584th-4095th)
1	0	1	1	11 (1024 blocks, protected block 3072nd-4095th)
1	1	0	0	12 (2048 blocks, protected block 2048th-4095th)
1	1	0	1	13 (4096 blocks, protected all)
1	1	1	0	14 (4096 blocks, protected all)
1	1	1	1	15 (4096 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	2Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th-1st)
0	0	1	1	3 (4 blocks, protected block 0th-3rd)
0	1	0	0	4 (8 blocks, protected block 0th-7th)
0	1	0	1	5 (16 blocks, protected block 0th-15th)
0	1	1	0	6 (32 blocks, protected block 0th-31st)
0	1	1	1	7 (64 blocks, protected block 0th-63rd)
1	0	0	0	8 (128 blocks, protected block 0th-127th)
1	0	0	1	9 (256 blocks, protected block 0th-255th)
1	0	1	0	10 (512 blocks, protected block 0th-511th)
1	0	1	1	11 (1024 blocks, protected block 0th-1023rd)
1	1	0	0	12 (2048 blocks, protected block 0th-2047th)
1	1	0	1	13 (4096 blocks, protected all)
1	1	1	0	14 (4096 blocks, protected all)
1	1	1	1	15 (4096 blocks, protected all)

6-2. Additional 8K-bit secured OTP

The secured OTP for unique identifier: to provide 8K-bit one-time program area for setting device unique serial number. Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 8K-bit secured OTP by entering secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 10. Security Register Definition"* for security register bit definition and *"Table 4. 8K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down by factory or customer, the corresponding range cannot be changed any more. While in secured OTP mode, array access is not allowed.

Table 4. 8K-bit Secured OTP Definition

Address range	Size	Lock-down
xxx000~xxx1FF	4096-bit	Determined by Customer
xxx200~xxx3FF	4096-bit	Determined by Factory

7. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

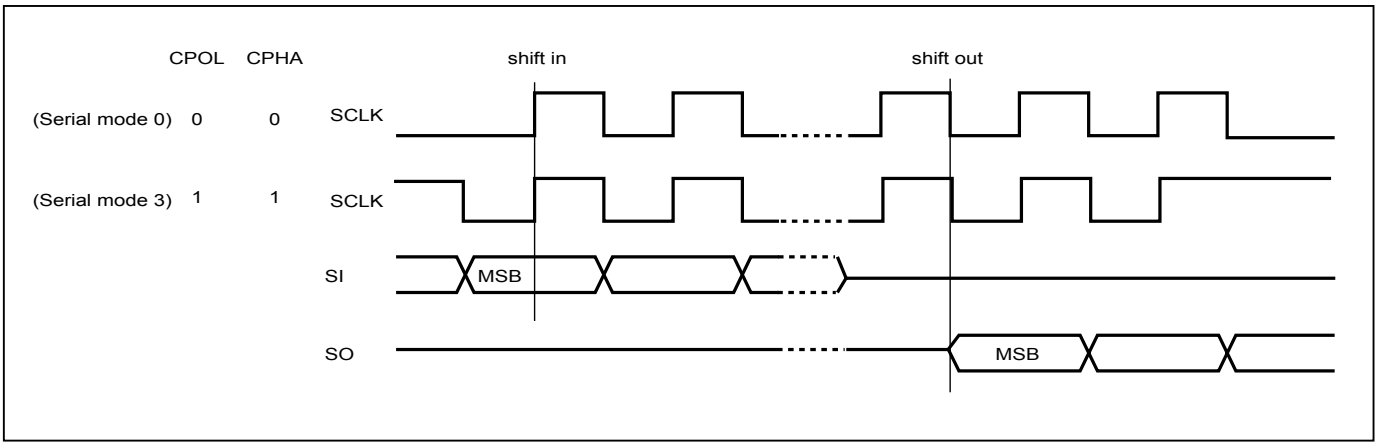
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".

5. For the following instructions: RDID, RDSR, RDSCUR, READ/READ4B, FAST_READ/FAST_READ4B, 2READ/2READ4B, DREAD/DREAD4B, 4READ/4READ4B, QREAD/QREAD4B, RDSFDP, RES, REMS, QPIID, RDDPB, RDSPB, RDLR, RDEAR, RDFBR, RDCR the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, PP/PP4B, 4PP/4PP4B, DP, ENSO, EXSO, WRSCUR, EN4B, EX4B, WPSEL, GBLK, GBULK, SUSPEND, RESUME, NOP, RSTEN, RST, EQIO, RSTQIO the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing (STR mode)

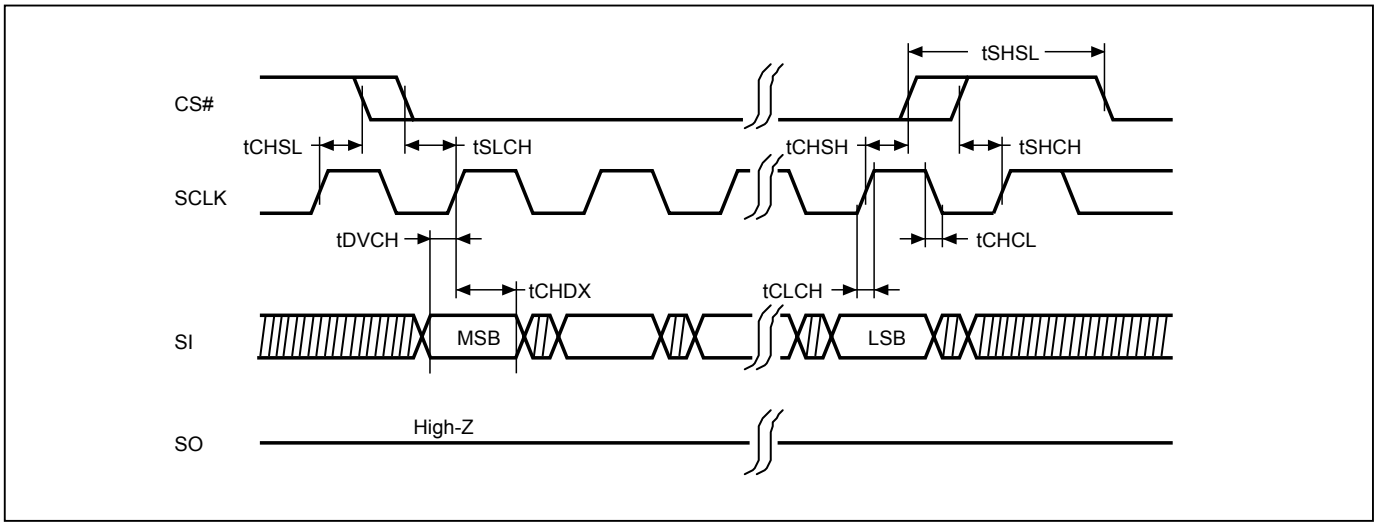


Figure 3. Serial Input Timing (DTR mode)

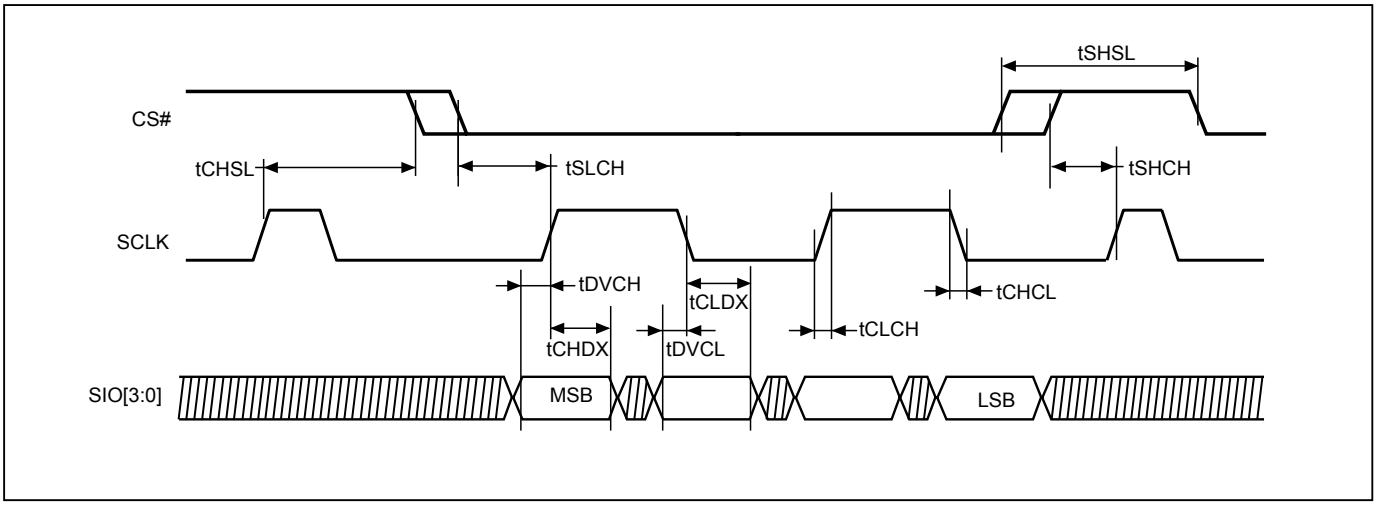


Figure 4. Output Timing (STR mode)

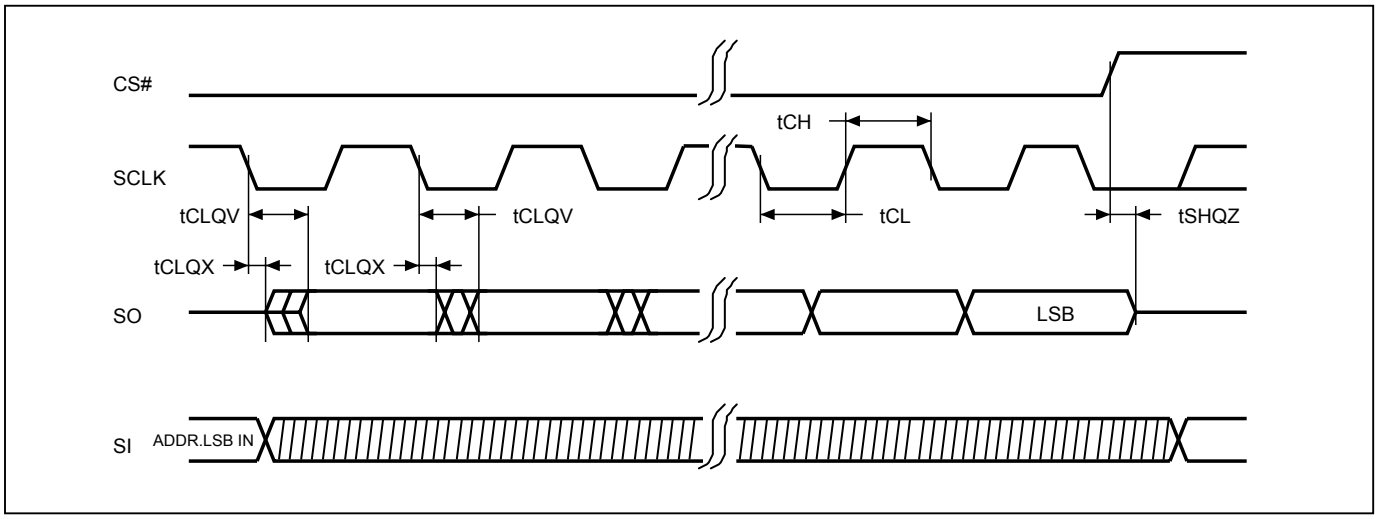
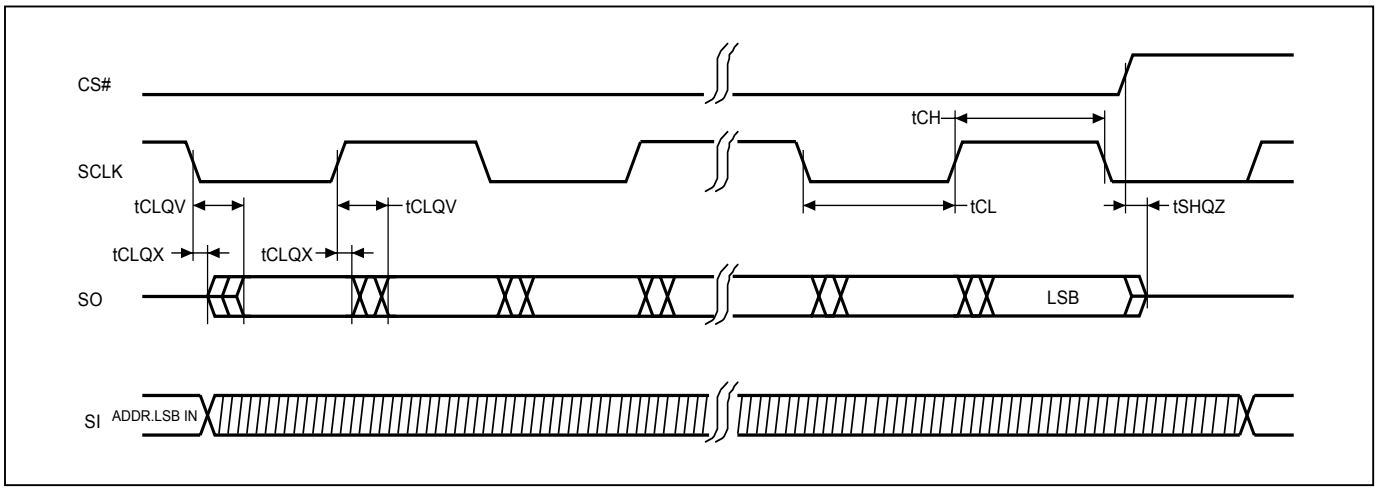


Figure 5. Output Timing (DTR mode)



7-1. 256Mb Address Protocol

The original 24 bit address protocol of Serial NOR Flash can only access density size below 128Mb. For the memory device of 256Mb and above, the 32bit address is requested for access higher memory size. The MX66U2G45G provides three different methods to access the whole density:

(1) Command entry 4-byte address mode:
Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register bit. After 4BYTE bit has been set, the number of address cycle become 32-bit.

(2) Extended Address Register (EAR):
configure the memory device into eight 128Mb segments to select which one is active through the EAR<0-3>.

(3) 4-byte Address Command Set:
When issuing 4-byte address command set, 4-byte address (A31-A0) is requested after the instruction code. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Enter 4-Byte Address Mode

In 4-byte Address mode, all instructions are 32-bits address clock cycles. By using EN4B and EX4B to enable and disable the 4-byte address mode.

When 4-byte address mode is enabled, the EAR<0-3> becomes "don't care" for all instructions requiring 4-byte address. The EAR function will be disabled when 4-byte mode is enabled.

Extended Address Register

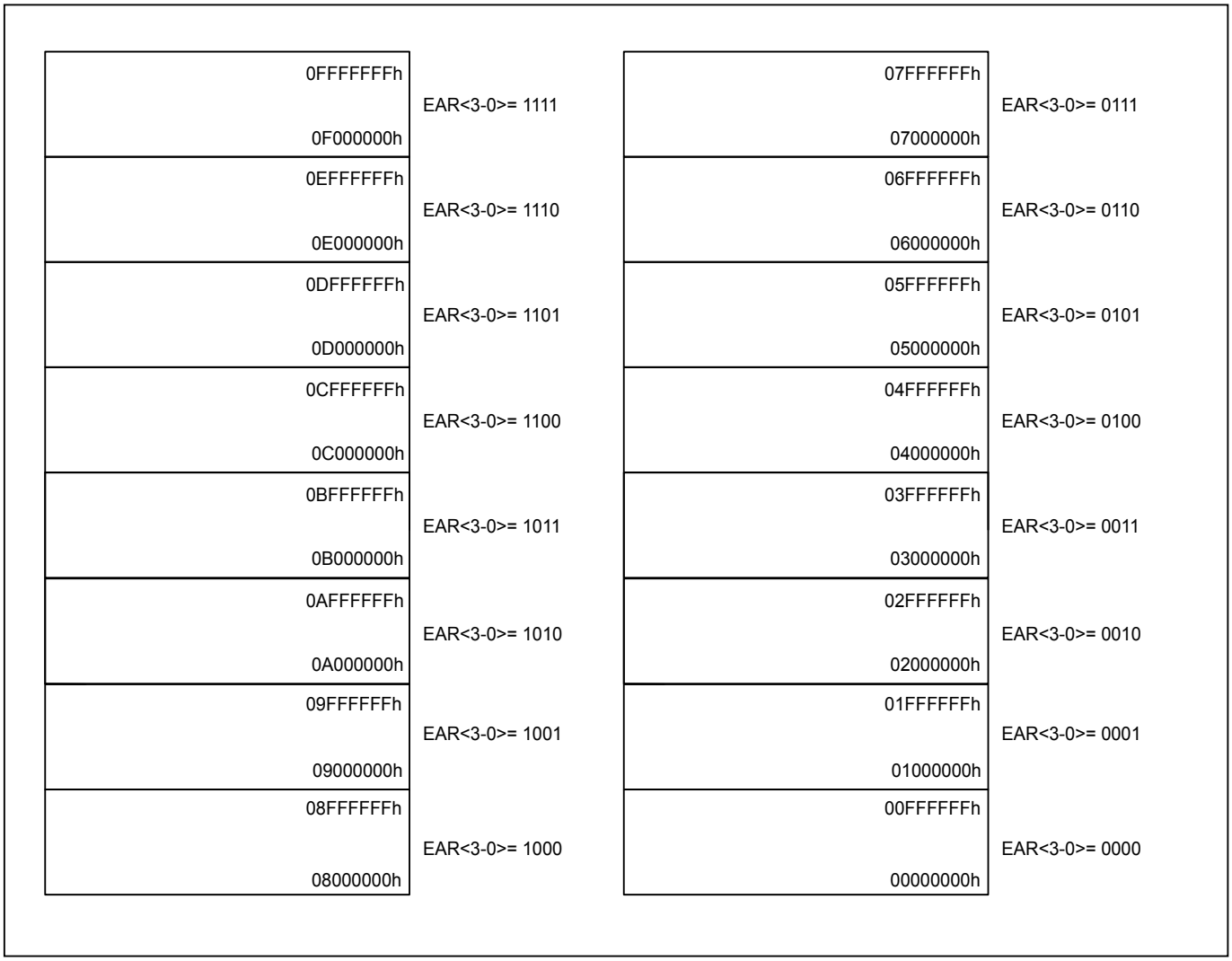
The device provides an 8-bit volatile register for extended Address Register: it identifies the extended address (A31~A24) above 128Mb density by using original 3-byte address.

Extended Address Register (EAR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A31	A30	A29	A28	A27	A26	A25	A24

For the MX66U2G45G the A31 to A28 are Don't Care. During EAR, reading these bits will read as 0. The bit 0 is default as "0".

Figure 6. EAR Operation Segments



When under EAR mode, Read, Program, Erase operates in the selected segment by using 3-byte address mode.

For the read operation, the whole array data can be continually read out with one command. Data output starts from the selected 128Mb block, but it can cross the boundary. When the last byte of the segment is reached, the next byte (in a continuous reading) is the first byte of the next segment. However, the EAR (Extended Address Register) value does not change. The random access reading can only be operated in the selected segment.

The Chip erase command will erase the whole chip and is not limited by EAR selected segment. However, the sector erase ,block erase , program operation are limited in selected segment and will not cross the boundary.

Figure 7. Write EAR Register (WREAR) Sequence (SPI Mode)

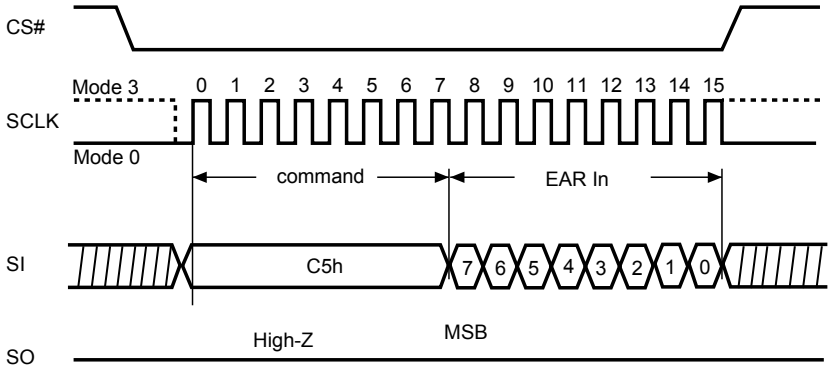


Figure 8. Write EAR Register (WREAR) Sequence (QPI Mode)

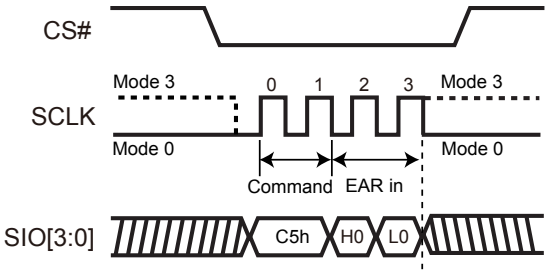


Figure 9. Read EAR (RDEAR) Sequence (SPI Mode)

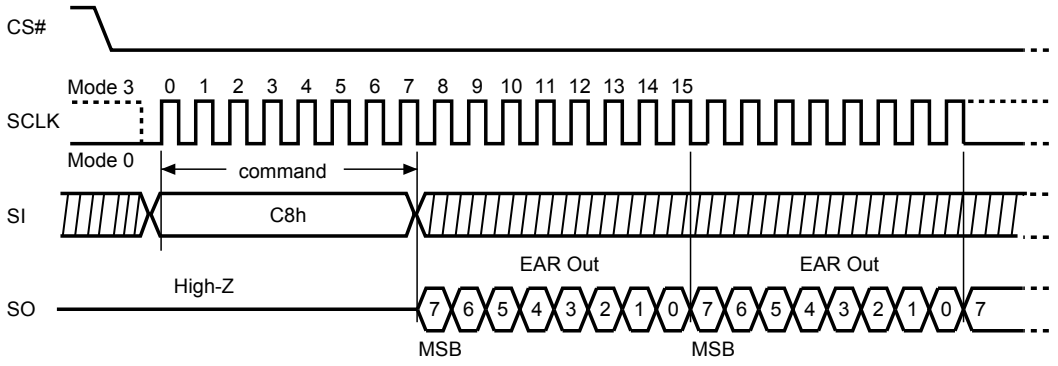
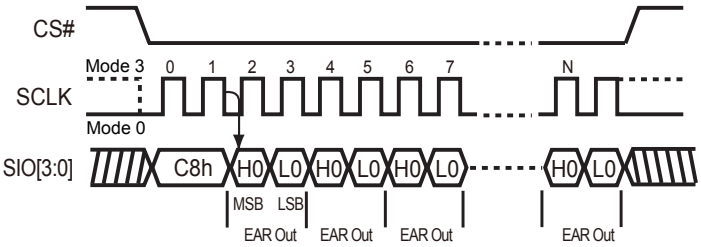


Figure 10. Read EAR (RDEAR) Sequence (QPI Mode)



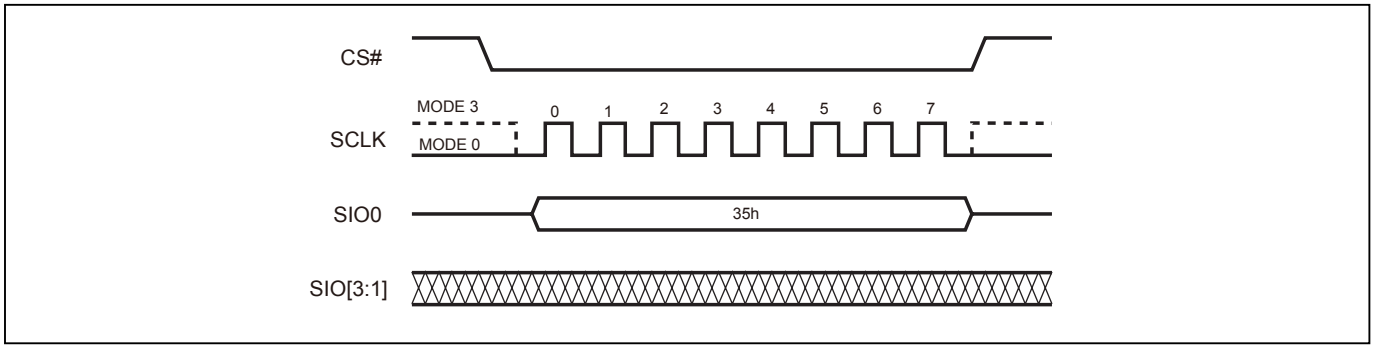
7-2. Quad Peripheral Interface (QPI) Read Mode

QPI protocol enables user to take full advantage of Quad I/O Serial NOR Flash by providing the Quad I/O interface in command cycles, address cycles and as well as data output cycles.

Enable QPI mode

By issuing command EQIO(35h), the QPI mode is enabled.

Figure 11. Enable QPI Sequence

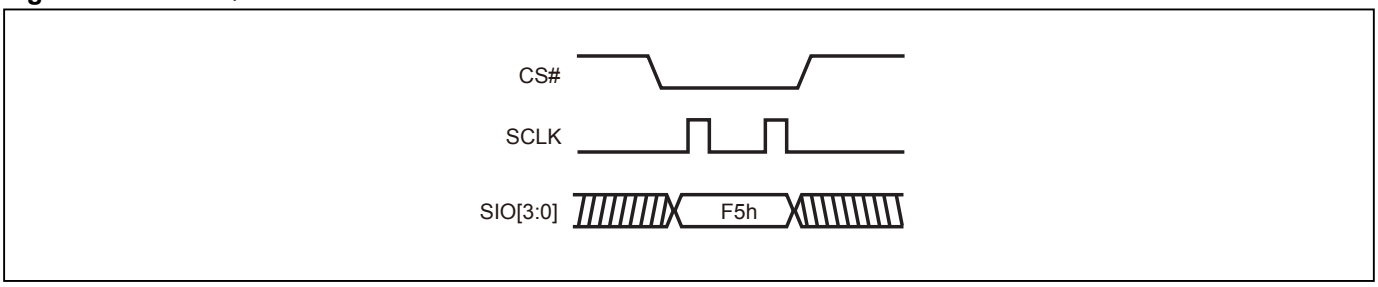


Reset QPI (RSTQIO)

To reset the QPI mode, the RSTQIO (F5h) command is required. After the RSTQIO command is issued, the device returns from QPI mode (4 I/O interface in command cycles) to SPI mode (1 I/O interface in command cycles).

Note:
For EQIO and RSTQIO commands, CS# high width has to follow "write spec" tSHSL for next instruction, as defined in *"Table 19. AC CHARACTERISTICS"*.

Figure 12. Reset QPI Mode



8. COMMAND SET

Table 5. Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read)	DREAD (1I 2O read)	4READ (4 I/O read)	QREAD (1I 4O read)	4DTRD (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	3/4	3/4
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)	ED (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	n bytes read out by Quad output until CS# goes high	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	3/4	3/4	3/4	3/4	3/4	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

* Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

Notes 2: Please note the address cycles above are based on 3-byte address mode. After enter 4-byte address mode by EN4B command, the address cycles will be increased to 4byte.

Table 6. Read/Write Array Commands (4 Byte Address Command Set)

Command (byte)	READ4B	FAST READ4B	2READ4B	DREAD4B	4READ4B	QREAD4B	4DTRD4B (Quad I/O DT Read)
Mode	SPI	SPI	SPI	SPI	SPI/QPI	SPI	SPI/QPI
Address Bytes	4	4	4	4	4	4	4
1st byte	13 (hex)	0C (hex)	BC (hex)	3C (hex)	EC (hex)	6C (hex)	EE (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte		Dummy*	Dummy*	Dummy*	Dummy*	Dummy*	Dummy*
Data Cycles							
Action	read data byte by 4 byte address	read data byte by 4 byte address	read data byte by 2 x I/O with 4 byte address	Read data byte by Dual Output with 4 byte address	read data byte by 4 x I/O with 4 byte address	Read data byte by Quad Output with 4 byte address	n bytes read out (Double Transfer Rate) by 4xI/O until CS# goes high

Command (byte)	PP4B	4PP4B	BE4B (block erase 64KB)	BE32K4B (block erase 32KB)	SE4B (Sector erase 4KB)
Mode	SPI/QPI	SPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	4	4	4	4	4
1st byte	12 (hex)	3E (hex)	DC (hex)	5C (hex)	21 (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte					
Data Cycles	1-256	1-256			
Action	to program the selected page with 4byte address	Quad input to program the selected page with 4byte address	to erase the selected (64KB) block with 4byte address	to erase the selected (32KB) block with 4byte address	to erase the selected (4KB) sector with 4byte address

Table 7. Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	RDEAR (read extended address register)	WREAR (write extended address register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	C8 (hex)	C5 (hex)
2nd byte					Values		
3rd byte					Values		
4th byte							
5th byte							
Data Cycles					1-2		1
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register	read extended address register	write extended address register

Command (byte)	WPSEL (Write Protect Selection)	EQIO (Enable QPI)	RSTQIO (Reset QPI)	EN4B (enter 4-byte mode)	EX4B (exit 4-byte mode)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)
Mode	SPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	68 (hex)	35 (hex)	F5 (hex)	B7 (hex)	E9 (hex)	B0 or 75 (hex)	30 or 7A (hex)
2nd byte							
3rd byte							
4th byte							
5th byte							
Data Cycles							
Action	to enter and enable individal block protect mode	Entering the QPI mode	Exiting the QPI mode	to enter 4-byte mode and set 4BYTE bit as "1"	to exit 4-byte mode and clear 4BYTE bit to be "0"		

Command (byte)	DP (Deep power down)	RDP (Release from deep power down)	SBL (Set Burst Length)	RDFBR (read fast boot register)	WRFBR (write fast boot register)	ESFBR (erase fast boot register)
Mode	SPI/QPI	SPI/QPI	SPI/QPI	SPI	SPI	SPI
1st byte	B9 (hex)	AB (hex)	C0 (hex)	16(hex)	17(hex)	18(hex)
2nd byte						
3rd byte						
4th byte						
5th byte						
Data Cycles				1-4	4	
Action	enters deep power down mode	release from deep power down mode	to set Burst length			

Table 8. ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	QPIID (QPI ID Read)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)
Mode	SPI	SPI/QPI	SPI	QPI	SPI/QPI	SPI/QPI	SPI/QPI
Address Bytes	0	0	0	0	3	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	AF (hex)	5A (hex)	B1 (hex)	C1 (hex)
2nd byte		x	x		ADD1		
3rd byte		x	x		ADD2		
4th byte			ADD1		ADD3		
5th byte					Dummy (8)		
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	ID in QPI interface	Read SFDP mode	to enter the secured OTP mode	to exit the secured OTP mode

Command (byte)	RDSCUR (read security register)	WRSCUR (write security register)	GBLK (gang block lock)	GBULK (gang block unlock)	WRLR (write Lock register)	RDLR (read Lock register)	WRSPB (SPB bit program)
Mode	SPI/QPI	SPI/QPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	0	0	0	0	0	4
1st byte	2B (hex)	2F (hex)	7E (hex)	98 (hex)	2C (hex)	2D (hex)	E3 (hex)
2nd byte							ADD1
3rd byte							ADD2
4th byte							ADD3
5th byte							ADD4
Data Cycles					2	2	
Action	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	whole chip write protect	whole chip unprotect			

Command (byte)	ESSPB (all SPB bit erase)	RDSPB (read SPB status)	WRDPB (write DPB register)	RDDPB (read DPB register)	RDPASS (read password register)	WRPASS (write password register)	PASSULK (password unlock)
Mode	SPI	SPI	SPI	SPI	SPI	SPI	SPI
Address Bytes	0	4	4	4	4	4	4
1st byte	E4 (hex)	E2 (hex)	E1 (hex)	E0 (hex)	27 (hex)	28 (hex)	29 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte		ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte		ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		ADD4	ADD4	ADD4	ADD4	ADD4	ADD4
6th byte					Dummy(8)(Note 4)		
Data Cycles		1	1	1	8	8	8
Action							

Table 9. Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
Mode	SPI/QPI	SPI/QPI	SPI/QPI
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

Note 1: ADD=00H will output the manufacturer ID first and ADD=01H will output device ID first.

Note 2: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.

Note 3: The RSTEN command must be executed before executing the RST command. If any other command is issued in-between RSTEN and RST, the RST command will be ignored.

Note 4: The number in parentheses after “ADD” or “Data” or “Dummy” stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in. Please note the number after "ADD" are based on 3-byte address mode, for 4-byte address mode, which will be increased.

9. REGISTER DESCRIPTION

9-1. Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit is a volatile bit that is set to “1” by the WREN instruction. WEL needs to be set to “1” before the device can accept program and erase instructions, otherwise the program and erase instructions are ignored. WEL automatically clears to “0” when a program or erase operation completes. To ensure that both WIP and WEL are “0” and the device is ready for the next program or erase operation, it is recommended that WIP be confirmed to be “0” before checking that WEL is also “0”. If a program or erase instruction is applied to a protected memory area, the instruction will be ignored and WEL will clear to “0”.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *Table 3*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit is a non-volatile bit with a factory default of “0”. When QE is “0”, Quad mode commands are ignored; pins WP#/SIO2 and NC/SIO3 function as WP# and NC, respectively. When QE is “1”, Quad mode is enabled and Quad mode commands are supported along with Single and Dual mode commands. Pins WP#/SIO2 and NC/SIO3 function as SIO2 and SIO3, respectively, and their alternate pin functions are disabled. Enabling Quad mode also disables the HPM feature.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only. The SRWD bit defaults to be "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disabled 0=status register write enabled	1=Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note 1: Please refer to the *"Table 3. Protected Area Sizes"*.

9-2. Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength (ODS2, ODS1, ODS0) bits are volatile bits, which indicate the output driver level (as defined in *Output Driver Strength Table*) of the device. To write the ODS bits requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

PBE bit
The Preamble Bit Enable (PBE) bit is a volatile bit. It is used to enable or disable the preamble bit data pattern output on dummy cycles. The PBE bit is defaulted as “0”, which means preamble bit is disabled. When it is set as “1”, the preamble bit will be enabled, and inputted into dummy cycles. To write the PBE bits requires the Write Status Register (WRSR) instruction to be executed.

4BYTE Indicator bit
By writing EN4B instruction, the 4BYTE bit may be set as "1" to access the address length of 32-bit for memory area of higher density (large than 128Mb). The default state is "0" as the 24-bit address mode. The 4BYTE bit may be cleared by power-off or writing EX4B instruction to reset the state to be "0".

Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DC1 (Dummy cycle 1)	DC0 (Dummy cycle 0)	4 BYTE	PBE (Preamble bit Enable)	TB (top/bottom selected)	ODS 2 (output driver strength)	ODS 1 (output driver strength)	ODS 0 (output driver strength)
(note 2)	(note 2)	0=3-byte address mode 1=4-byte address mode (Default=0)	0=Disable 1=Enable	0=Top area protect 1=Bottom area protect (Default=0)	(note 1)	(note 1)	(note 1)
volatile bit	volatile bit	volatile bit	volatile bit	OTP	volatile bit	volatile bit	volatile bit

Note 1: see *"Output Driver Strength Table"*
Note 2: see *"Dummy Cycle and Frequency Table (MHz)"*

Output Driver Strength Table

ODS2	ODS1	ODS0	Description	Note
0	0	0	146 Ohms	Impedance at VCC/2 (Typical)
0	0	1	76 Ohms	
0	1	0	52 Ohms	
0	1	1	41 Ohms	
1	0	0	34 Ohms	
1	0	1	30 Ohms	
1	1	0	26 Ohms	
1	1	1	24 Ohms (Default)	

Dummy Cycle and Frequency Table (MHz)

DC[1:0]	Numbers of Dummy clock cycles	Fast Read	Dual Output Fast Read	Quad Output Fast Read
00 (default)	8	133	133	133
01	6	133	133	104
10	8	133	133	133
11	10	166	166	166

DC[1:0]	Numbers of Dummy clock cycles	Dual IO Fast Read
00 (default)	4	84
01	6	104
10	8	133
11	10	166

DC[1:0]	Numbers of Dummy clock cycles	Quad IO Fast Read	Quad I/O DTR Read
00 (default)	6	84	52
01	4	70	42
10	8	104	66
11	10	133	102

9-3. Security Register

The definition of the Security Register bits is as below:

Write Protection Selection bit. Please reference to "*Write Protection Selection bit*"

Erase Fail bit. The Erase Fail bit shows the status of last Erase operation. The bit will be set to "1" if the erase operation failed or the erase region was protected. It will be automatically cleared to "0" if the next erase operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit shows the status of the last Program operation. The bit will be set to "1" if the program operation failed or the program region was protected. It will be automatically cleared to "0" if the next program operation succeeds. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the secured OTP area is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the Secured OTP area cannot be updated any more. While it is in secured OTP mode, main array access is not allowed.

Table 10. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
0=normal WP mode 1=individual mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0 = non-factory lock 1 = factory lock
Non-volatile bit (OTP)	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

10. COMMAND DESCRIPTION

10-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP/PP4B, 4PP/4PP4B, SE/SE4B, BE32K/BE32K4B, BE/BE4B, CE, and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

Figure 13. Write Enable (WREN) Sequence (SPI Mode)

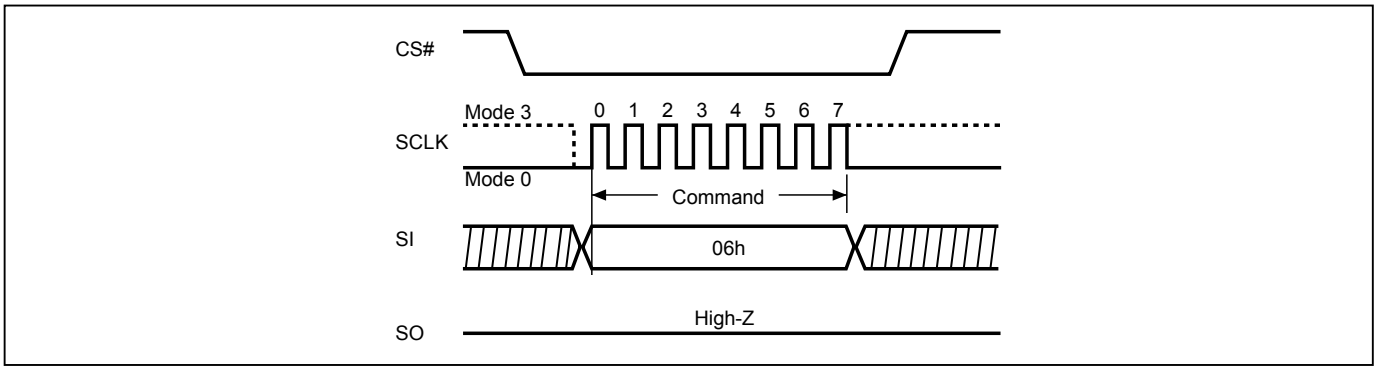
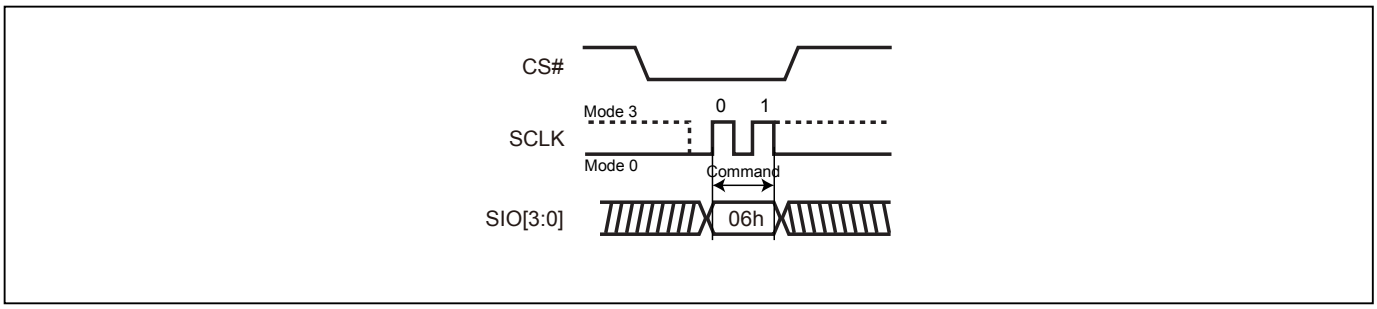


Figure 14. Write Enable (WREN) Sequence (QPI Mode)



10-2. Write Disable (WRDI)

The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care in SPI mode.

The WEL bit is reset by following situations:

- Power-up
- Reset# pin driven low
- WRDI command completion
- WRSR command completion
- PP/PP4B command completion
- 4PP/4PP4B command completion
- SE/SE4B command completion
- BE32K/BE32K4B command completion
- BE/BE4B command completion
- CE command completion
- PGM/ERS Suspend command completion
- Softreset command completion
- WRSCUR command completion
- WPSEL command completion
- GBLK command completion
- GBULK command completion
- WREAR command completion
- WRLR command completion
- WRSPB command completion
- ESSPB command completion
- WRDPB command completion
- WRFBR command completion
- ESFBR command completion

Figure 15. Write Disable (WRDI) Sequence (SPI Mode)

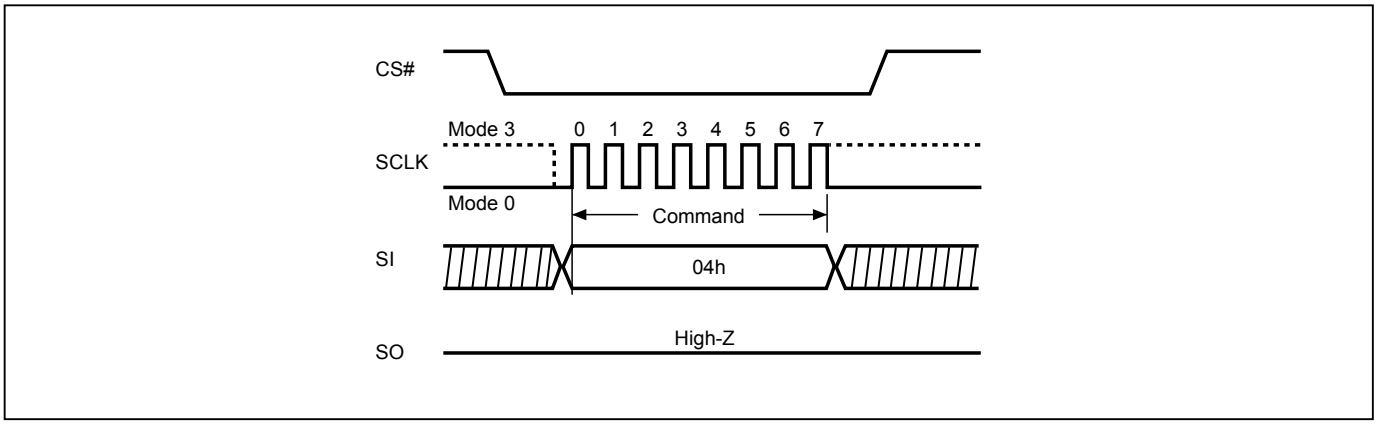
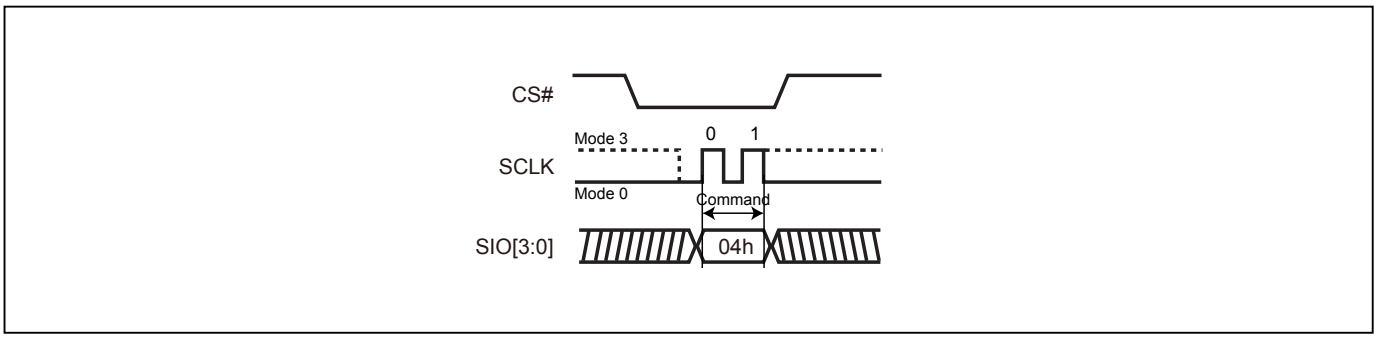


Figure 16. Write Disable (WRDI) Sequence (QPI Mode)



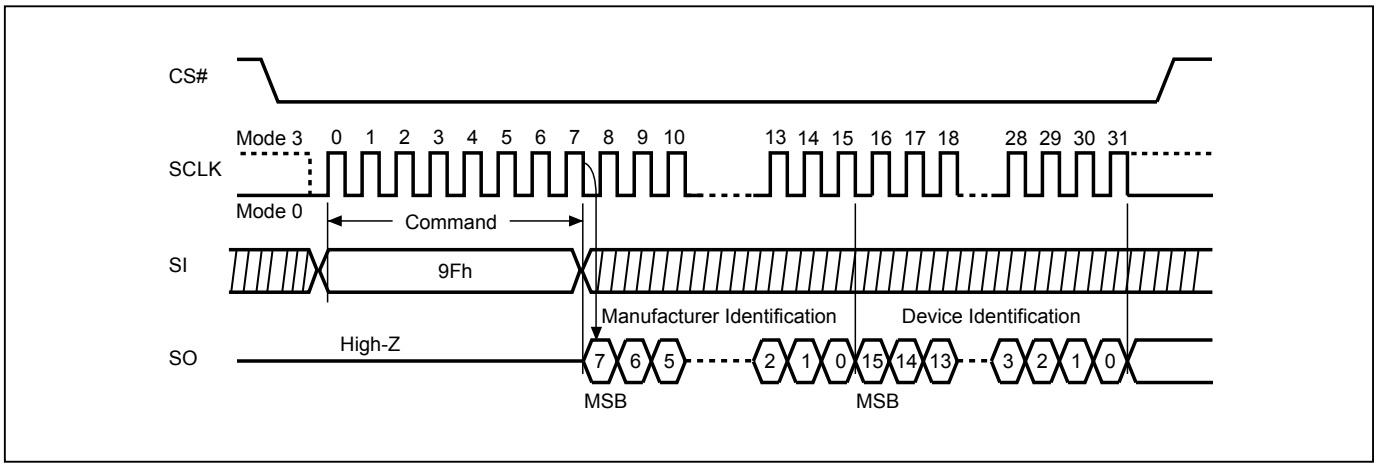
10-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 11. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 17. Read Identification (RDID) Sequence (SPI mode only)



10-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 19. AC CHARACTERISTICS"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode. Reset# pin goes low will release the Flash from deep power down mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *Table 11* ID Definitions. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 18. Read Electronic Signature (RES) Sequence (SPI Mode)

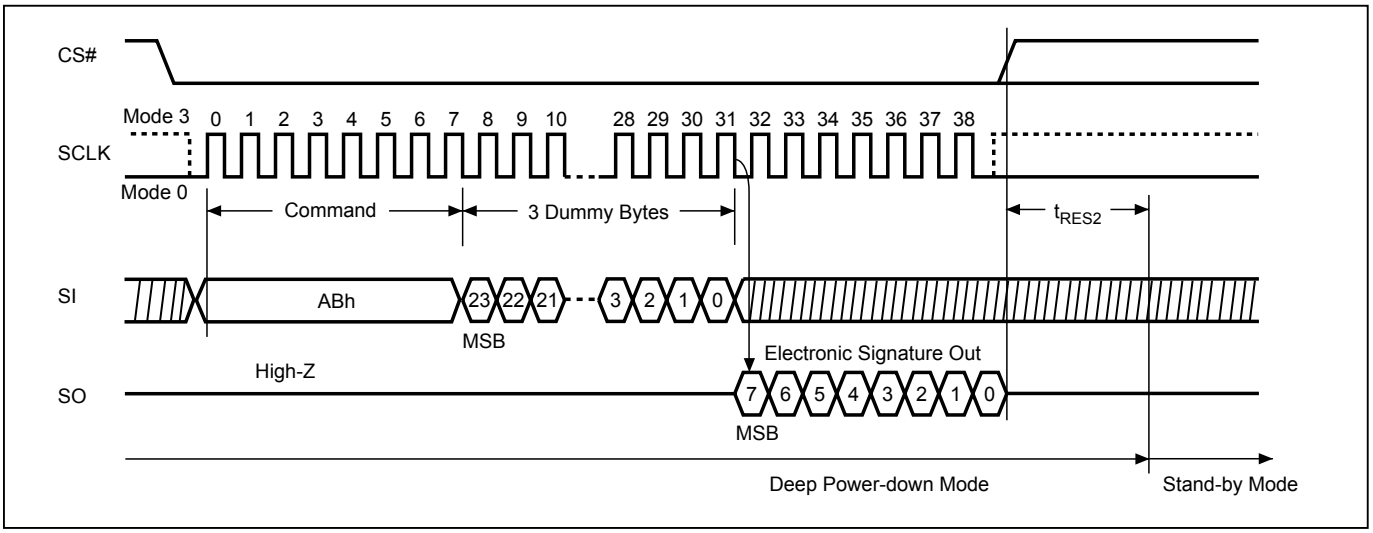


Figure 19. Read Electronic Signature (RES) Sequence (QPI Mode)

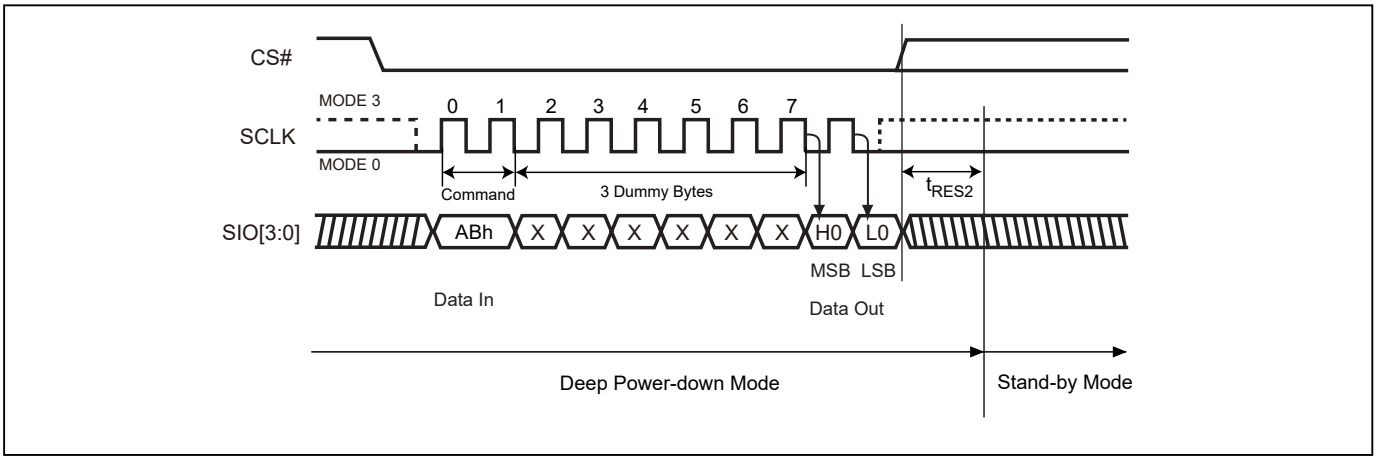


Figure 20. Release from Deep Power-down (RDP) Sequence (SPI Mode)

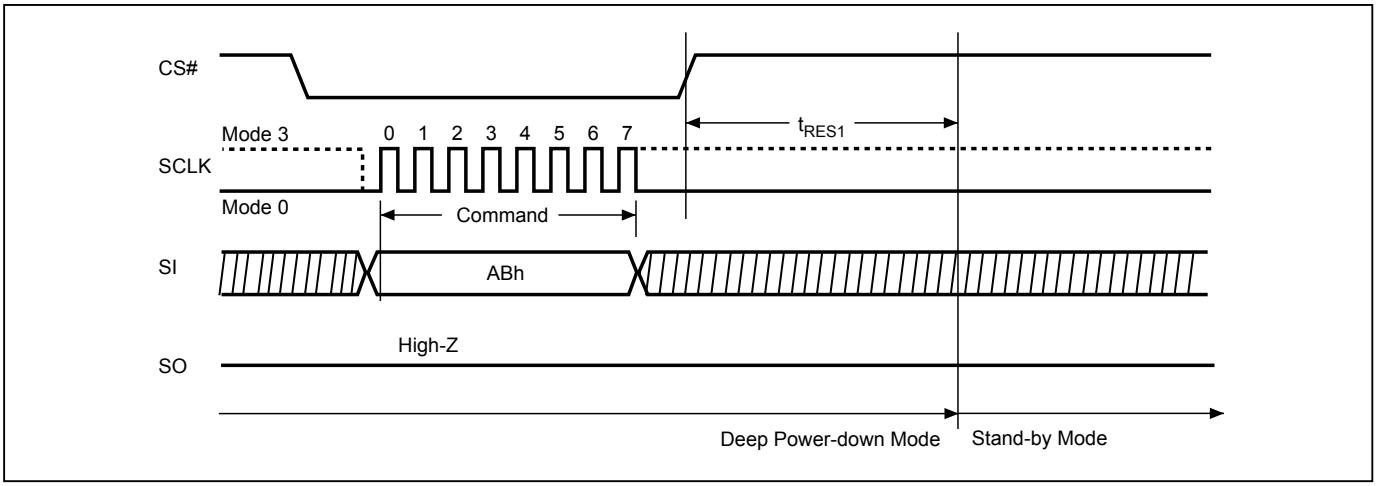
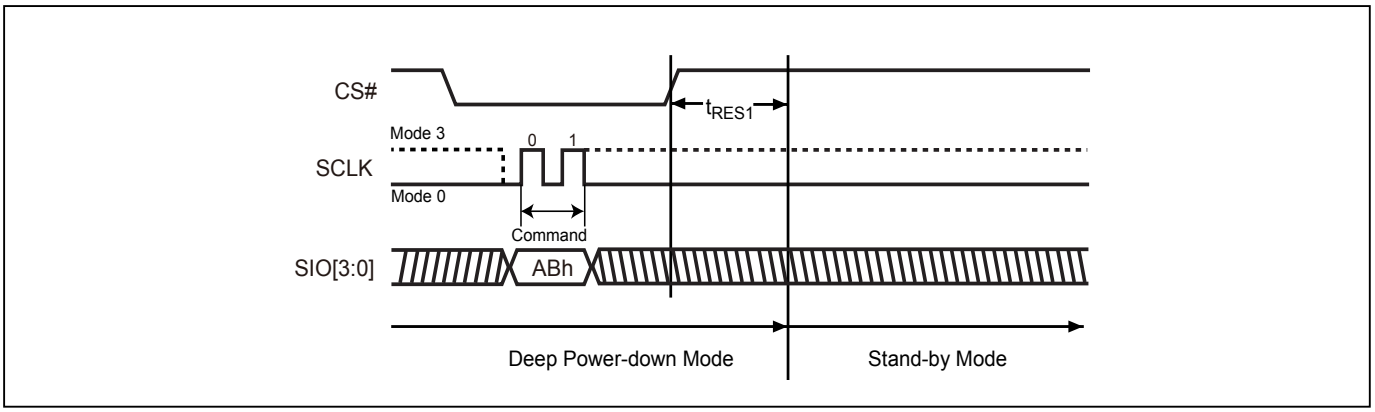


Figure 21. Release from Deep Power-down (RDP) Sequence (QPI Mode)

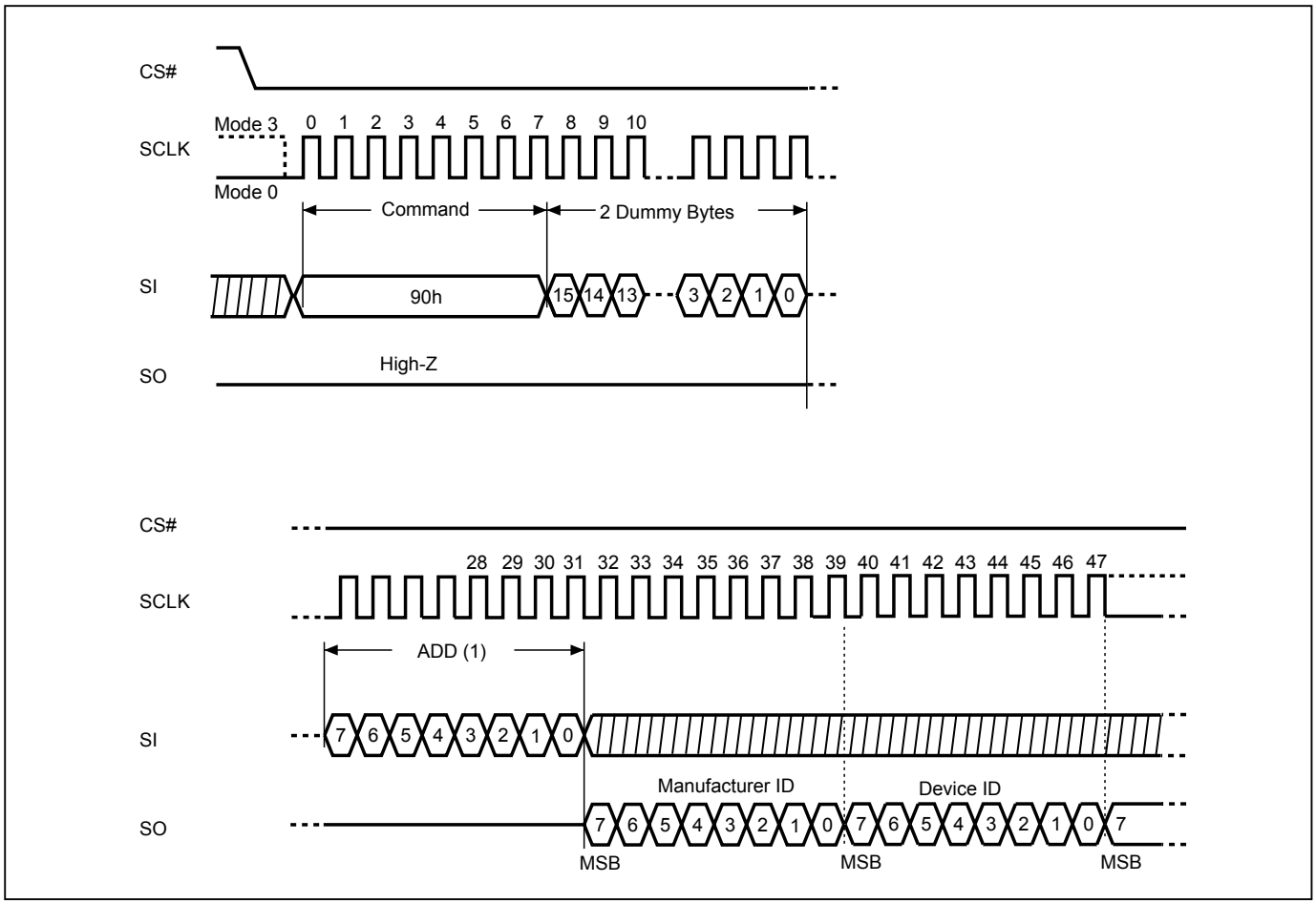


10-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction returns both the JEDEC assigned manufacturer ID and the device ID. The Device ID values are listed in *Table 11* of ID Definitions.

The REMS instruction is initiated by driving the CS# pin low and sending the instruction code "90h" followed by two dummy bytes and one address byte (A7~A0). After which the manufacturer ID for Macronix (C2h) and the device ID are shifted out on the falling edge of SCLK with the most significant bit (MSB) first. If the address byte is 00h, the manufacturer ID will be output first, followed by the device ID. If the address byte is 01h, then the device ID will be output first, followed by the manufacturer ID. While CS# is low, the manufacturer and device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 22. Read Electronic Manufacturer & Device ID (REMS) Sequence (SPI Mode only)



Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

10-6. QPI ID Read (QPIID)

User can execute this QPIID Read instruction to identify the Device ID and Manufacturer ID. The sequence of issue QPIID instruction is CS# goes low→sending QPI ID instruction→Data out on SO→CS# goes high. Most significant bit (MSB) first.

After the command cycle, the device will immediately output data on the falling edge of SCLK. The manufacturer ID, memory type, and device ID data byte will be output continuously, until the CS# goes high.

Table 11. ID Definitions

Command Type		MX66U2G45G		
RDID	9Fh	Manufacturer ID	Memory type	Memory density
		C2	25	3C
RES	ABh	Electronic ID		
		3C		
REMS	90h	Manufacturer ID	Device ID	
		C2	3C	
QPIID	AFh	Manufacturer ID	Memory type	Memory density
		C2	25	3C

10-7. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 23. Read Status Register (RDSR) Sequence (SPI Mode)

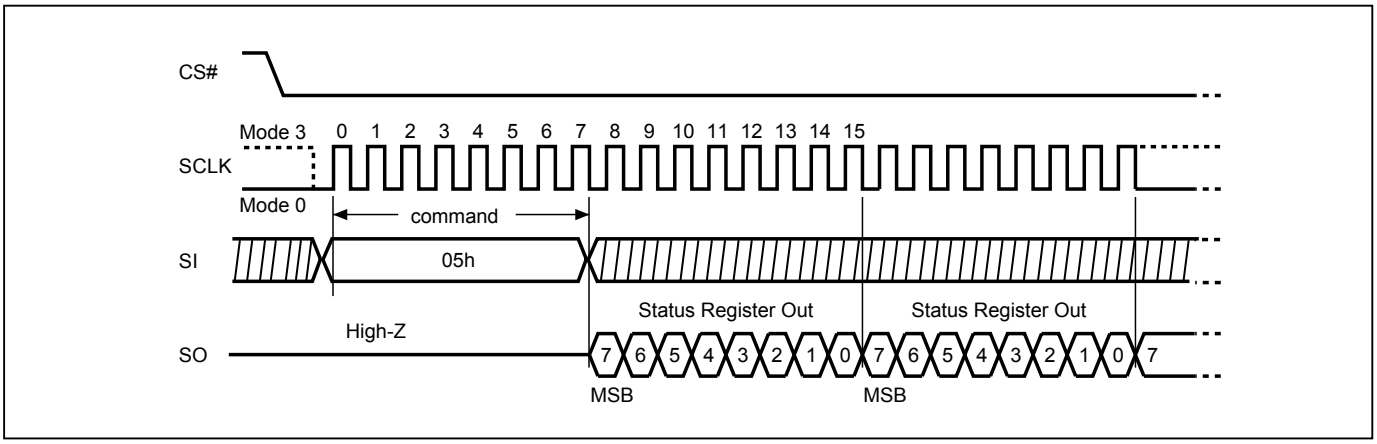
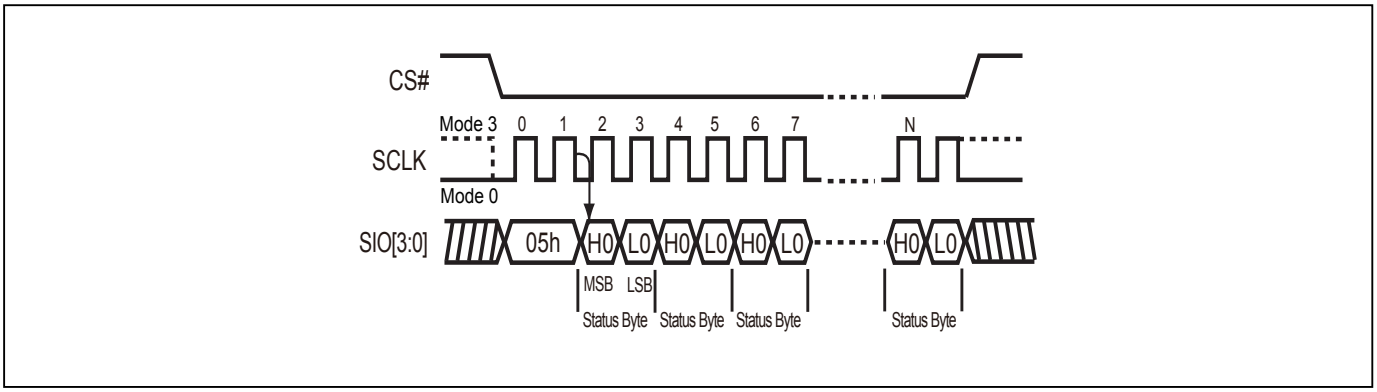


Figure 24. Read Status Register (RDSR) Sequence (QPI Mode)



10-8. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 25. Read Configuration Register (RDCR) Sequence (SPI Mode)

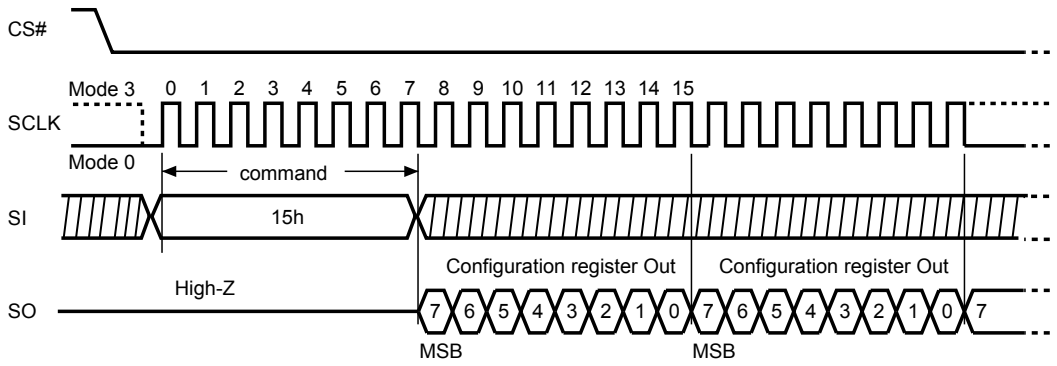
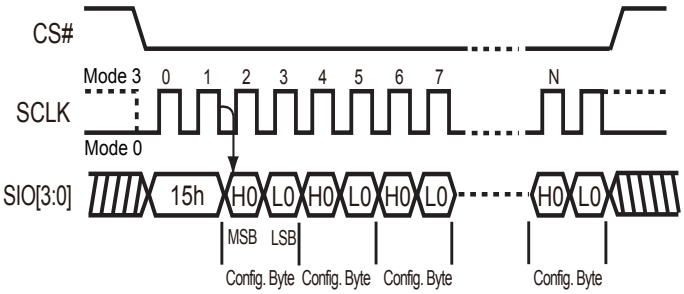


Figure 26. Read Configuration Register (RDCR) Sequence (QPI Mode)



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 27. Program/Erase flow with read array data

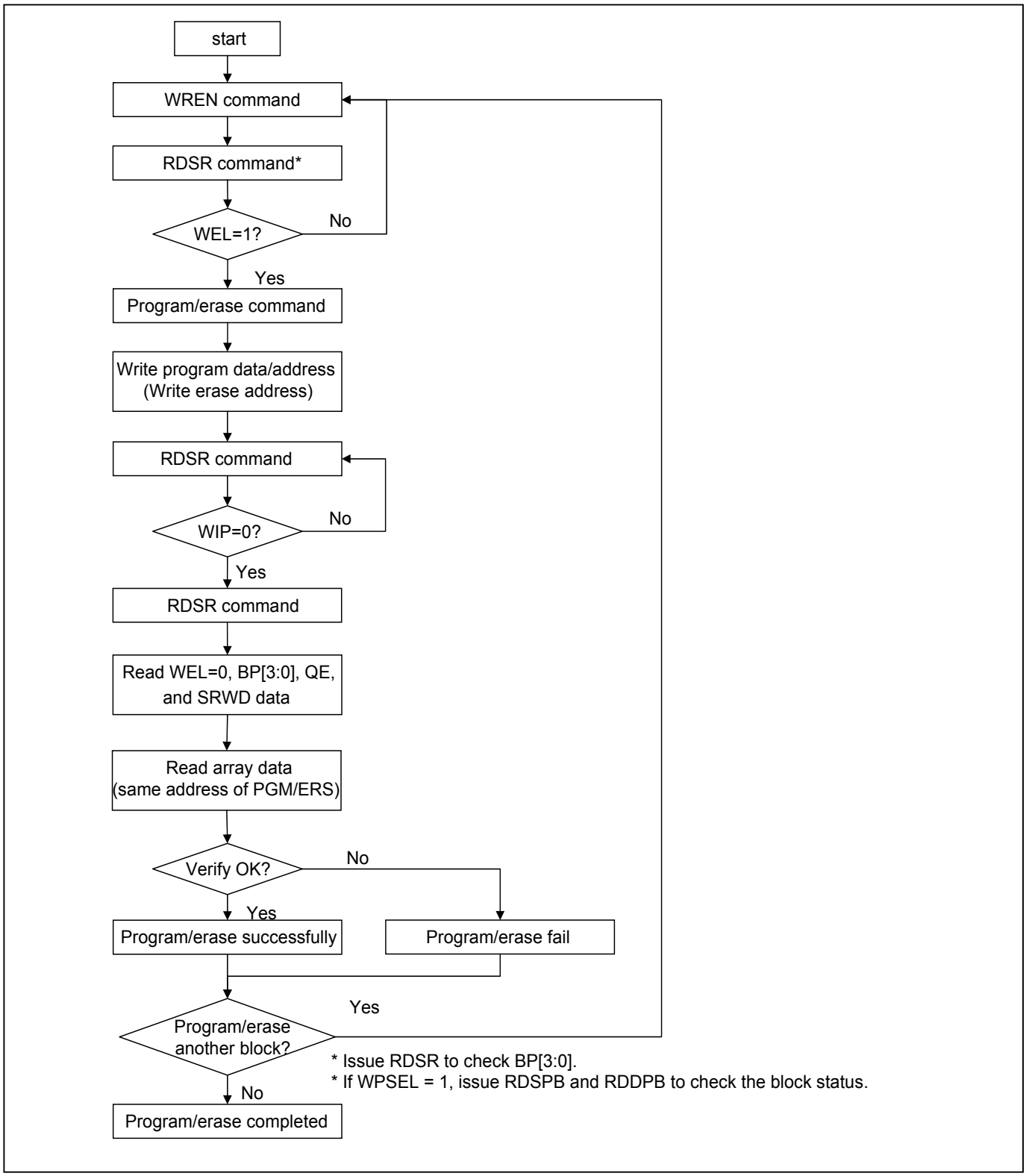
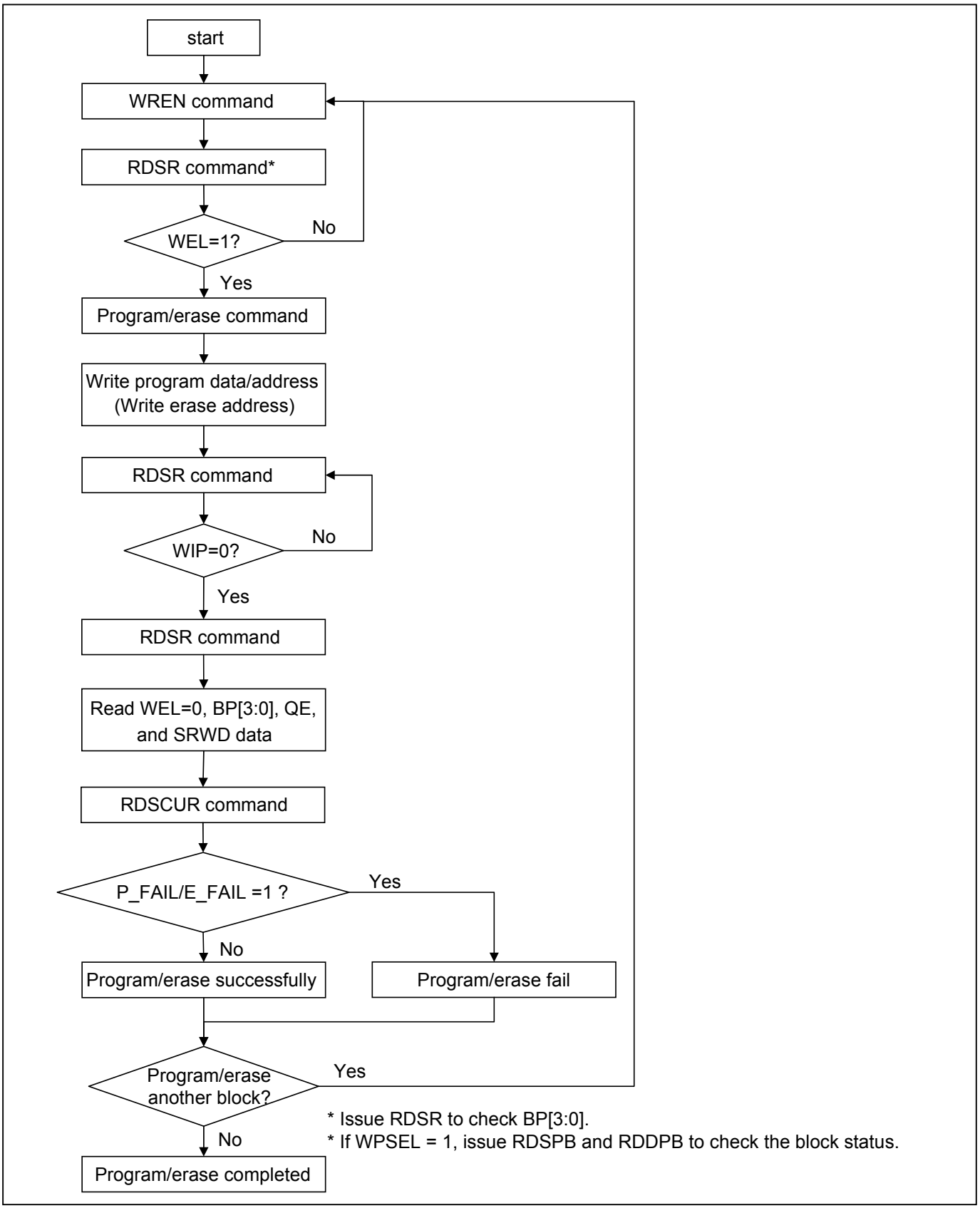


Figure 28. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



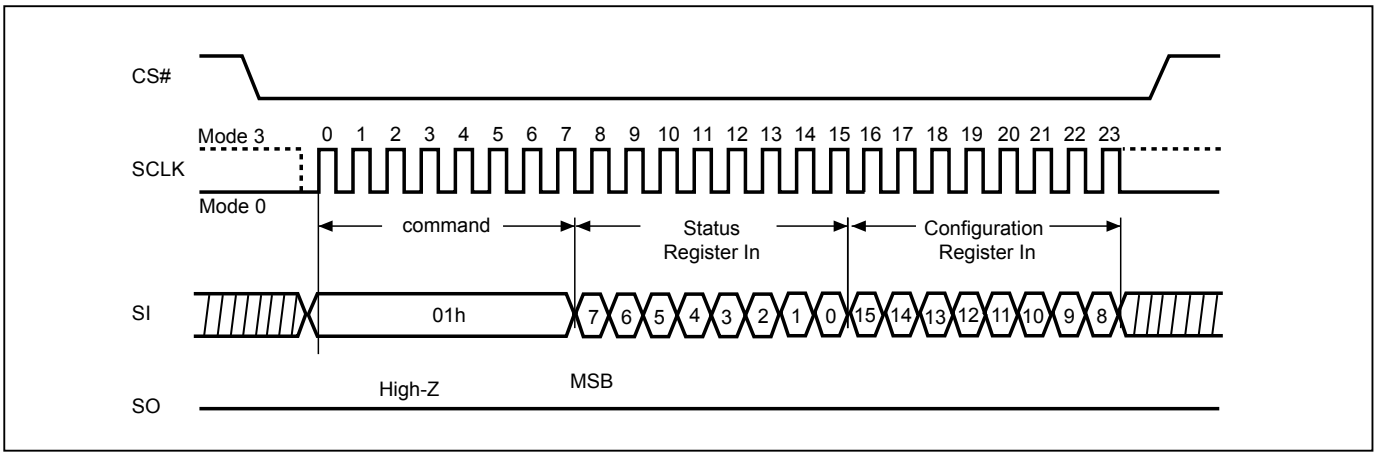
10-9. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *Table 3*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

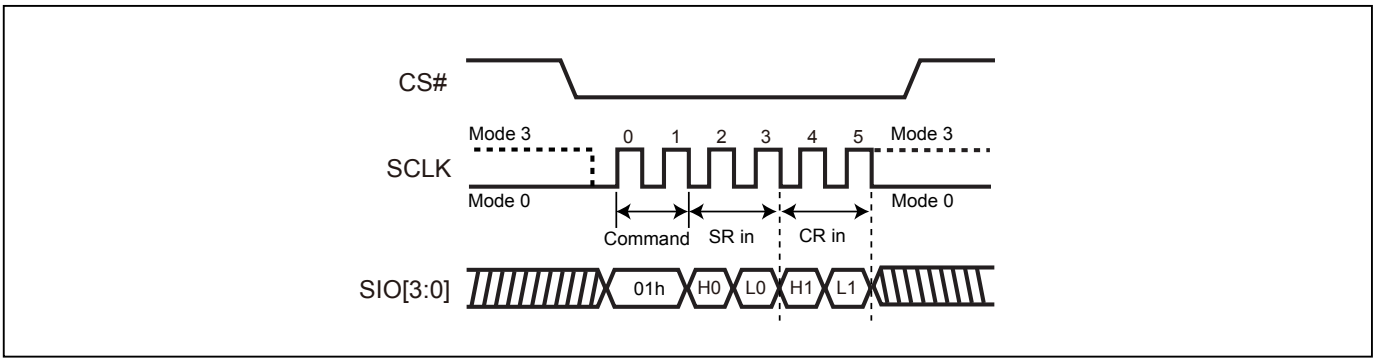
The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 29. Write Status Register (WRSR) Sequence (SPI Mode)



Note : The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Figure 30. Write Status Register (WRSR) Sequence (QPI Mode)



Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM)

Note:

If SRWD bit=1 but WP#/SIO2 is low, it is impossible to write the Status Register even if the WEL bit has previously been set. It is rejected to write the Status Register and not be executed.

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and T/B bit and hardware protected mode by the WP#/SIO2 to against data modification.

Note:

To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered. If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0 and T/B bit.
If the system enter QPI or set QE=1, the feature of HPM will be disabled.

Table 12. Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note:

1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *Table 3*.

Figure 31. WRSR flow

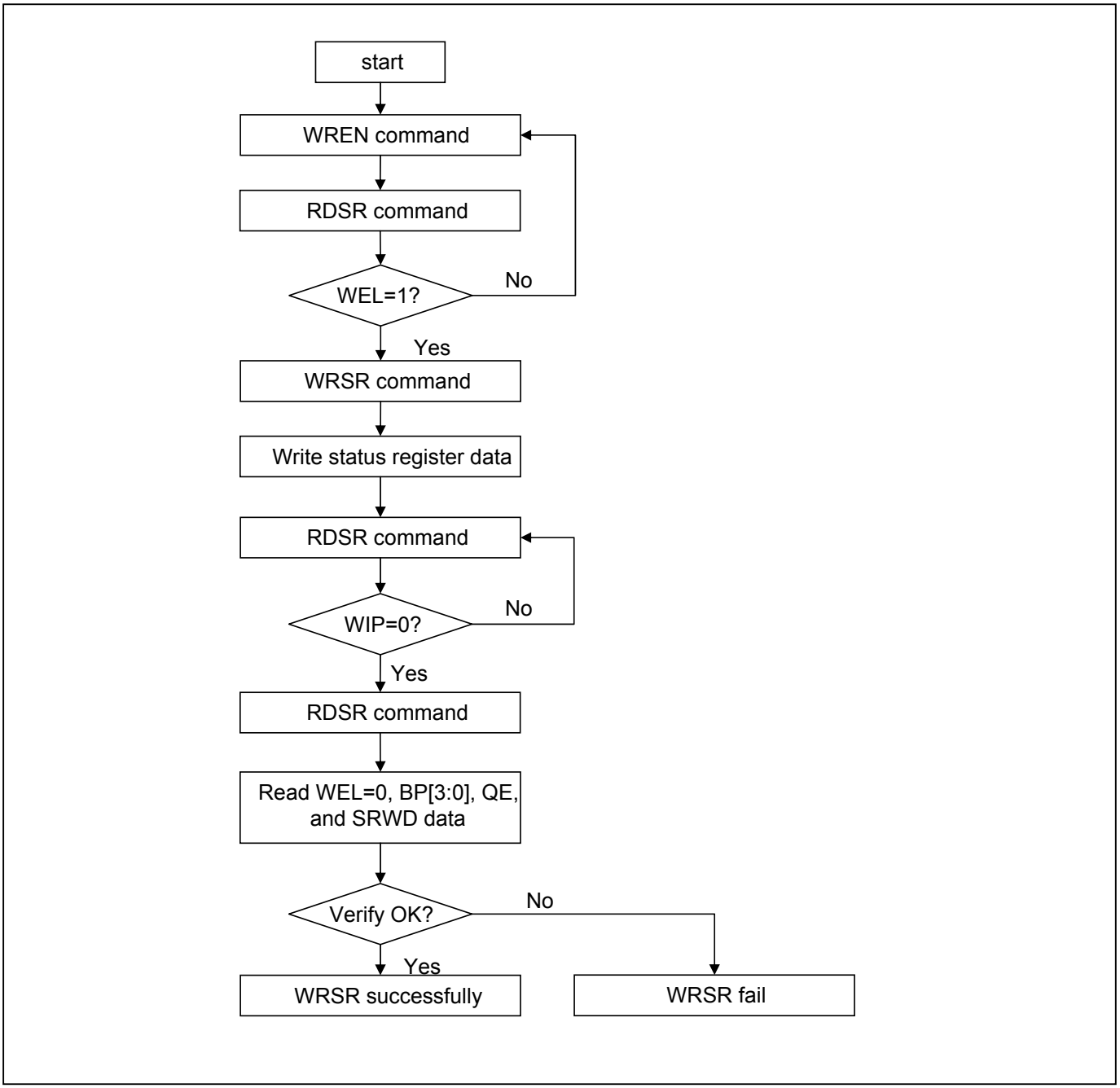
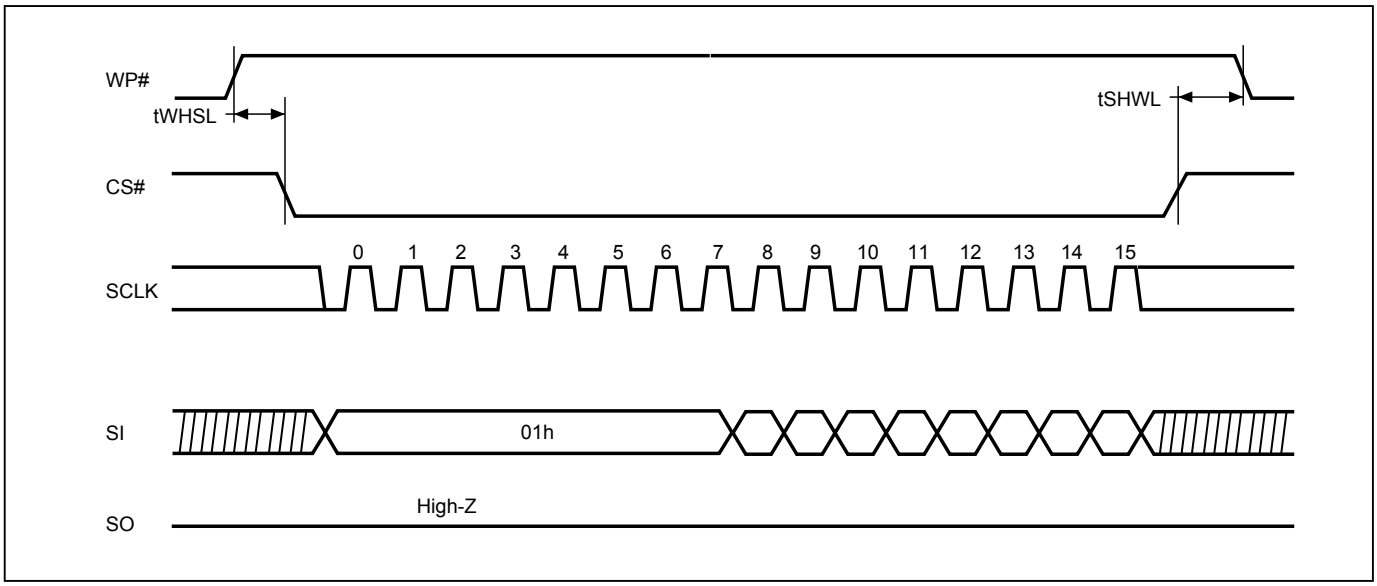


Figure 32. WP# Setup Timing and Hold Timing during WRSR when SRWD=1



Note: WP# must be kept high until the embedded operation finish.

10-10. Enter 4-byte mode (EN4B)

The EN4B instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit5 (4BYTE bit) of Configuration Register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. There are three methods to exit the 4-byte mode: writing exit 4-byte mode (EX4B) instruction, Reset or power-off.

All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The following command don't support 4bye address: RDSFDP, RES and REMS.

The sequence of issuing EN4B instruction is: CS# goes low → sending EN4B instruction to enter 4-byte mode(automatically set 4BYTE bit as "1") → CS# goes high.

10-11. Exit 4-byte mode (EX4B)

The EX4B instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the EX4B instruction, the bit5 (4BYTE bit) of Configuration Register will be cleared to be "0" to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low → sending EX4B instruction to exit 4-byte mode (automatically clear the 4BYTE bit to be "0") → CS# goes high.

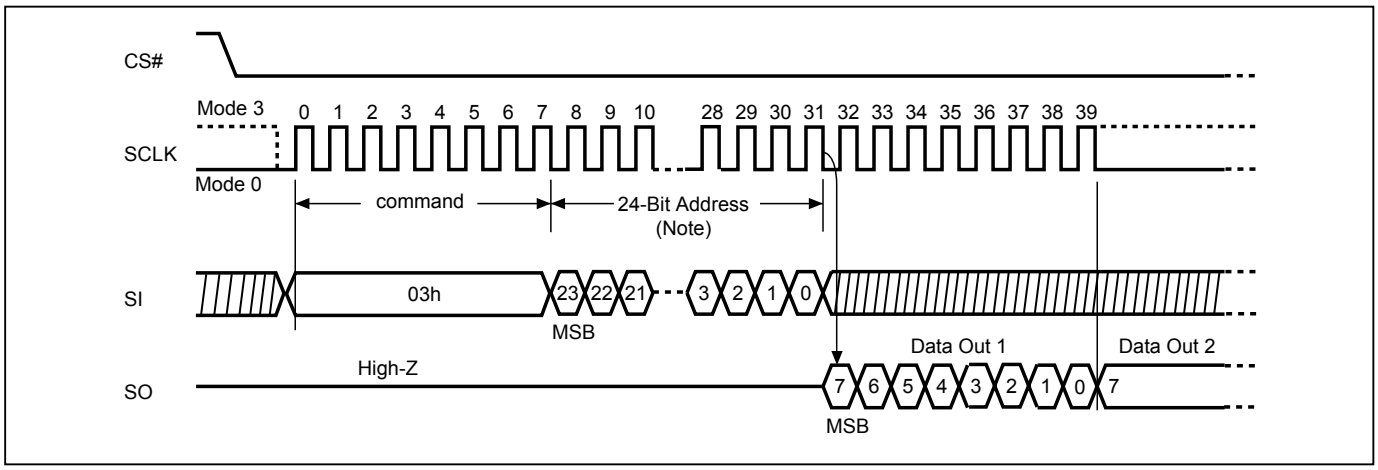
10-12. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte or 4-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 33. Read Data Bytes (READ) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-13. Read Data Bytes at Higher Speed (FAST_READ)

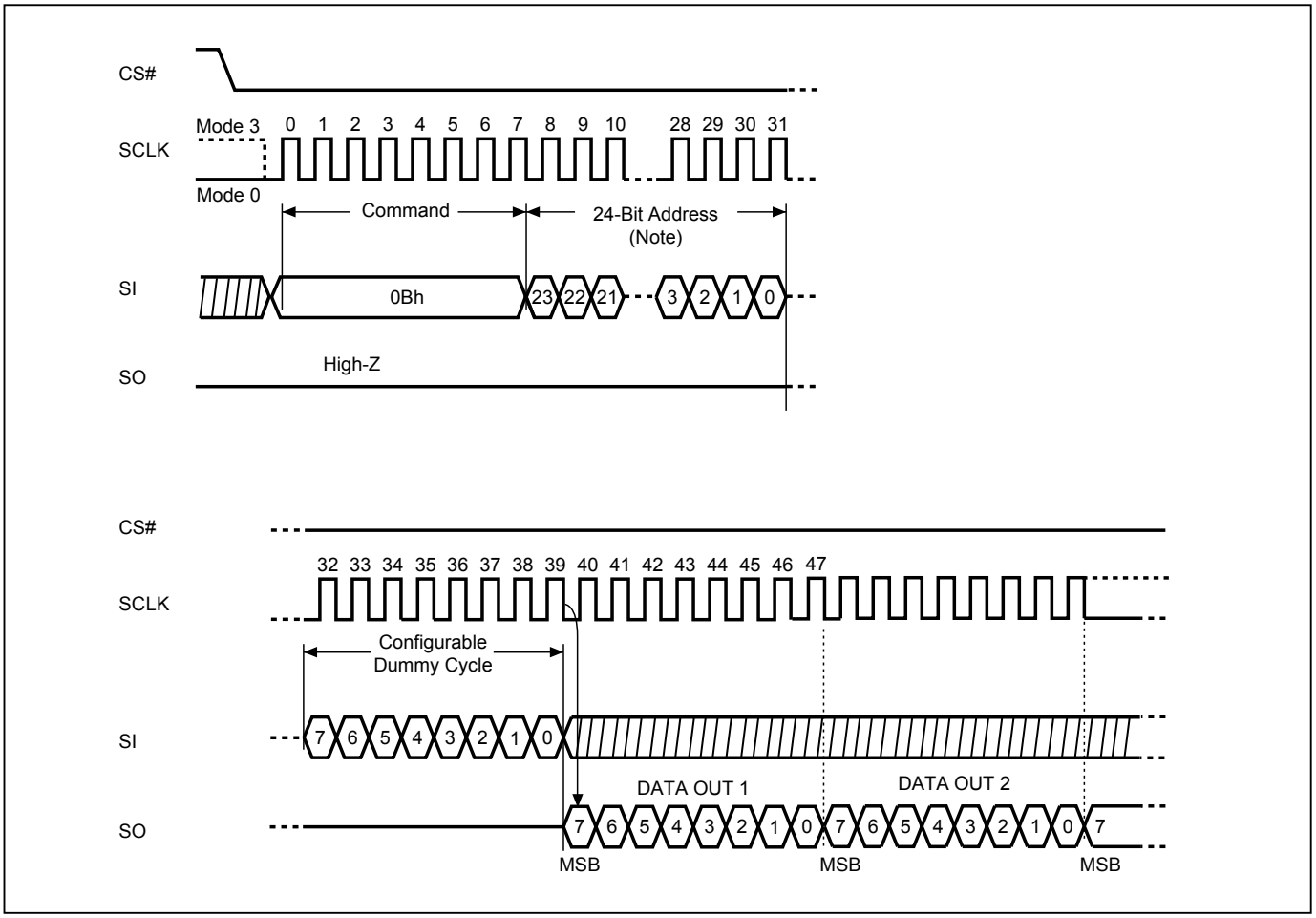
The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

Read on SPI Mode The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte or 4-byte address on SI→ 8 dummy cycles (default)→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 34. Read at Higher Speed (FAST_READ) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-14. Dual Output Read Mode (DREAD)

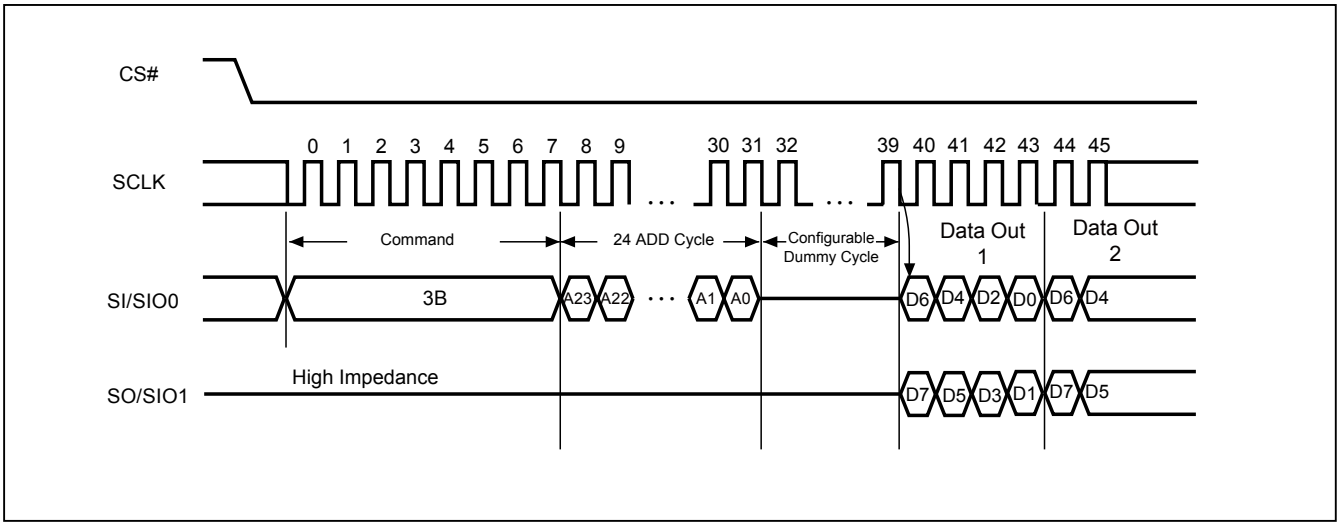
The DREAD instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing DREAD instruction is: CS# goes low→ sending DREAD instruction→3-byte or 4-byte address on SIO0→ 8 dummy cycles (default) on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 35. Dual Read Mode Sequence



Notes:
1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-15. 2 x I/O Read Mode (2READ)

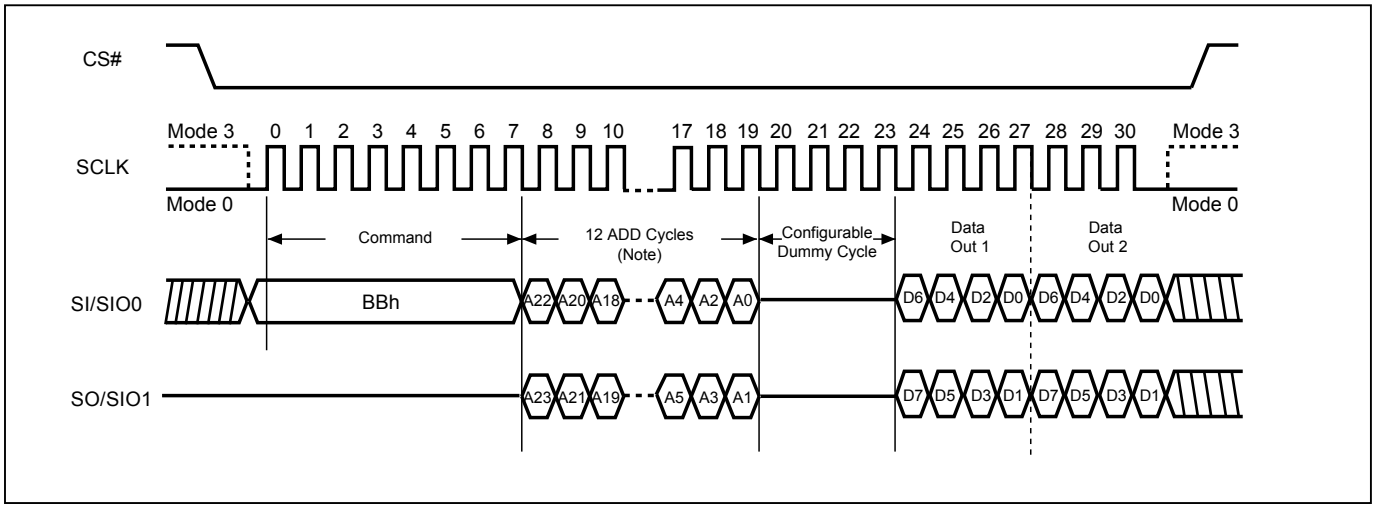
The 2READ instruction enable double throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 3-byte or 4-byte address interleave on SIO1 & SIO0→ 4 dummy cycles (default) on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 36. 2 x I/O Read Mode Sequence (SPI Mode only)



Notes:
1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-16. Quad Read Mode (QREAD)

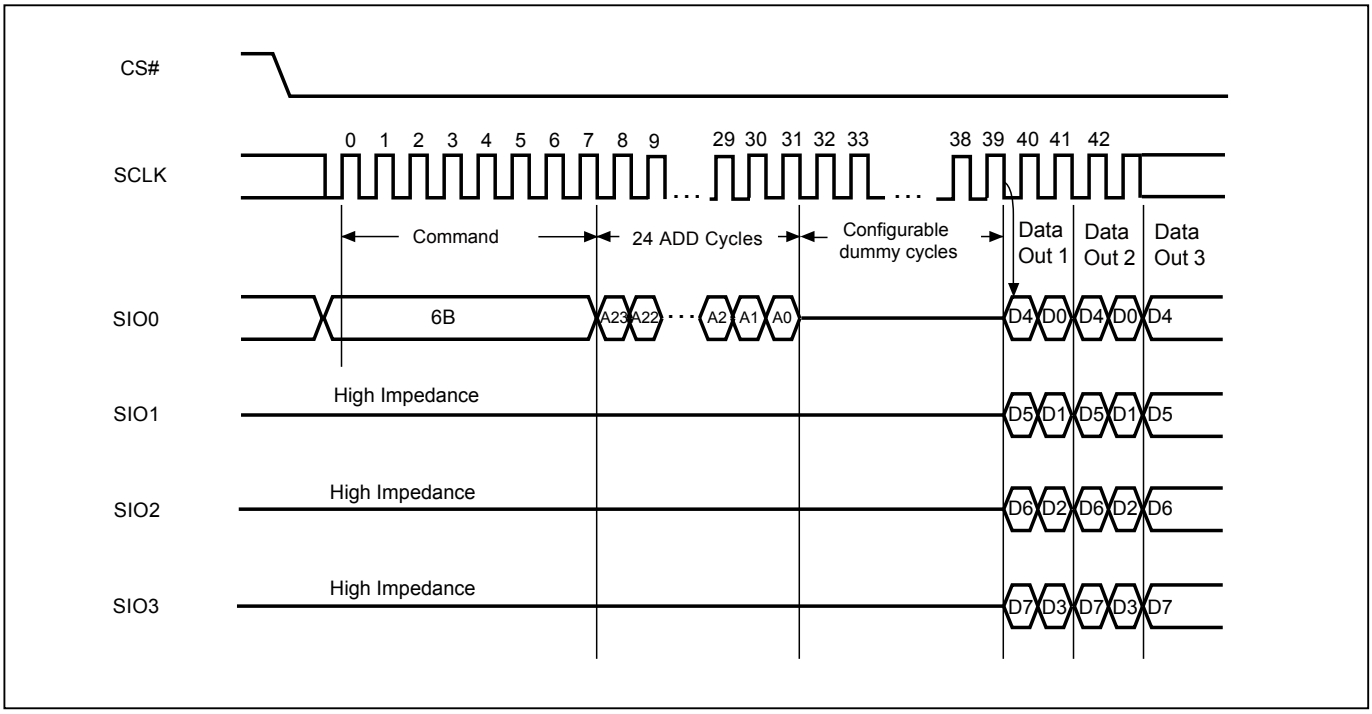
The QREAD instruction enable quad throughput of Serial NOR Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte or 4-byte address on SI → 8 dummy cycle (Default) → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 37. Quad Read Mode Sequence



Notes:
1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

10-17. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4READ instruction. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

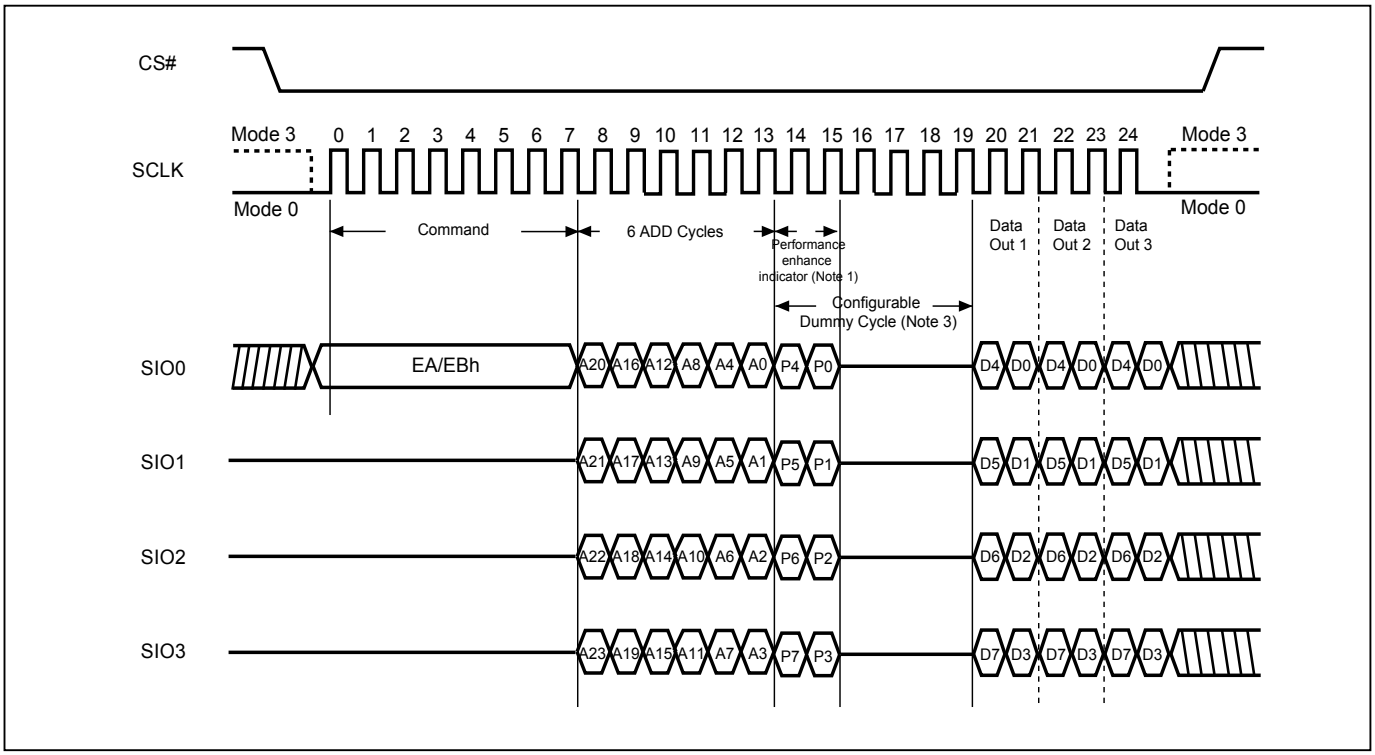
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

4 x I/O Read on SPI Mode (4READ) The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

4 x I/O Read on QPI Mode (4READ) The 4READ instruction also support on QPI command mode. The sequence of issuing 4READ instruction QPI mode is: CS# goes low→ sending 4READ instruction→ 3-byte or 4-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles (Default) →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

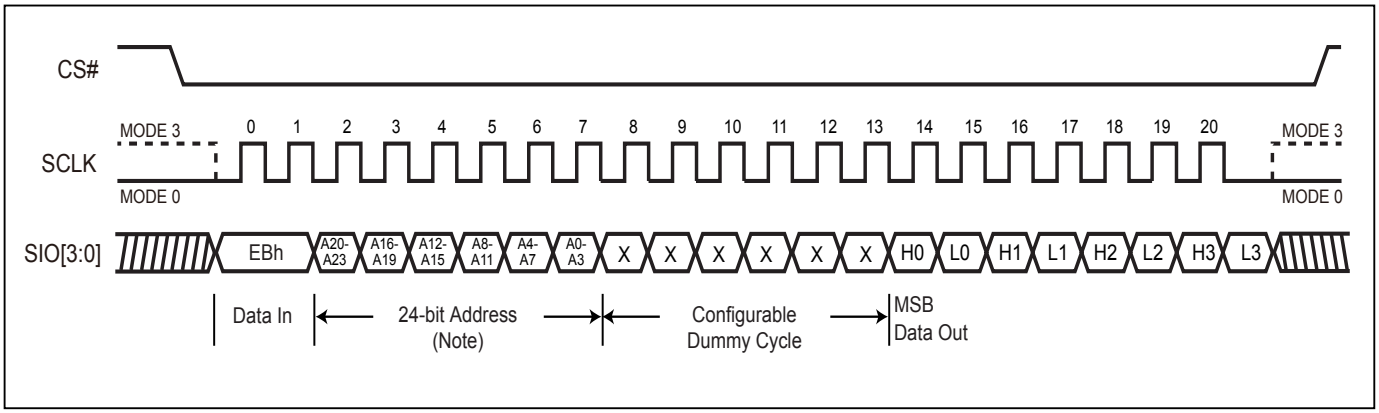
While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 38. 4 x I/O Read Mode Sequence (SPI Mode)



Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 39. 4 x I/O Read Mode Sequence (QPI Mode)



Notes:
1. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

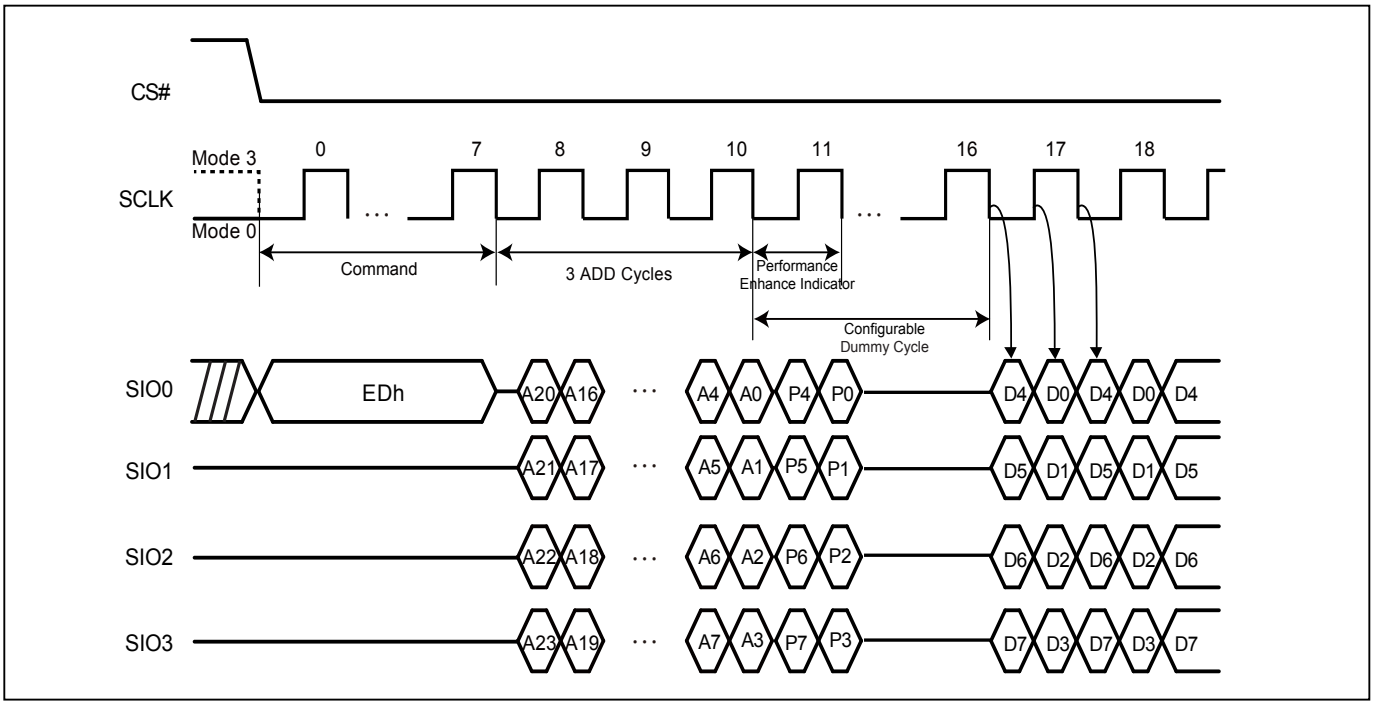
10-18. 4 x I/O Double Transfer Rate Read Mode (4DTRD)

The 4DTRD instruction enables Double Transfer Rate throughput on quad I/O of Serial NOR Flash in read mode. A Quad Enable (QE) bit of status Register must be set to "1" before sending the 4DTRD instruction. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of SCLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of SCLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4DTRD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4DTRD instruction, the following address/ dummy/data out will perform as 8-bit instead of previous 1-bit.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

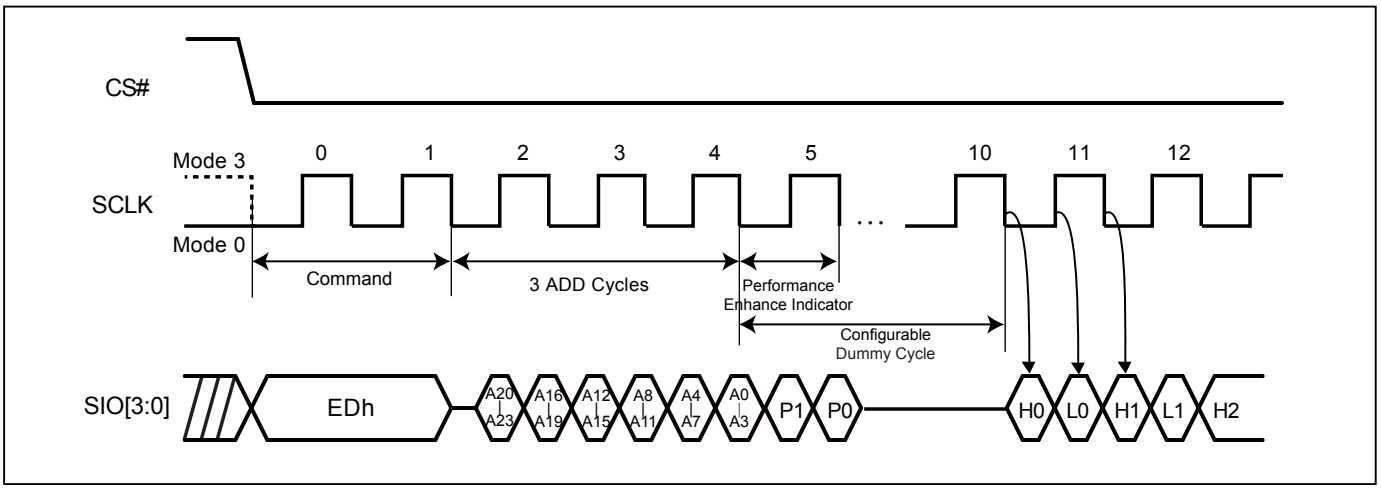
While Program/Erase/Write Status Register cycle is in progress, 4DTRD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 40. Fast Quad I/O DT Read (4DTRD) Sequence (SPI Mode)



Notes:
1. Hi-impedance is inhibited for this clock cycle.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) will result in entering the performance enhance mode.
3. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.
4. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 41. Fast Quad I/O DT Read (4DTRD) Sequence (QPI Mode)



Notes:
1. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit 7 (DC0 & DC1) setting in configuration register.

10-19. Preamble Bit

The Preamble Bit data pattern supports system/memory controller to determine valid window of data output more easily and improve data capture reliability while the flash memory is running in high frequency.

Preamble Bit data pattern can be enabled or disabled by setting the bit4 of Configuration register (Preamble bit Enable bit). Once the CR<4> is set, the preamble bit is inputted into dummy cycles.

Enabling preamble bit will not affect the function of enhance mode bit. In Dummy cycles, performance enhance mode bit still operates with the same function. Preamble bit will output after performance enhance mode bit.

The preamble bit is a fixed 8-bit data pattern (00110100). While dummy cycle number reaches 10, the complete 8 bits will start to output right after the performance enhance mode bit. While dummy cycle is not sufficient of 10 cycles, the rest of the preamble bits will be cut. For example, 8 dummy cycles will cause 6 preamble bits to output, and 6 dummy cycles will cause 4 preamble bits to output.

Figure 42. SDR 1I/O (10DC)

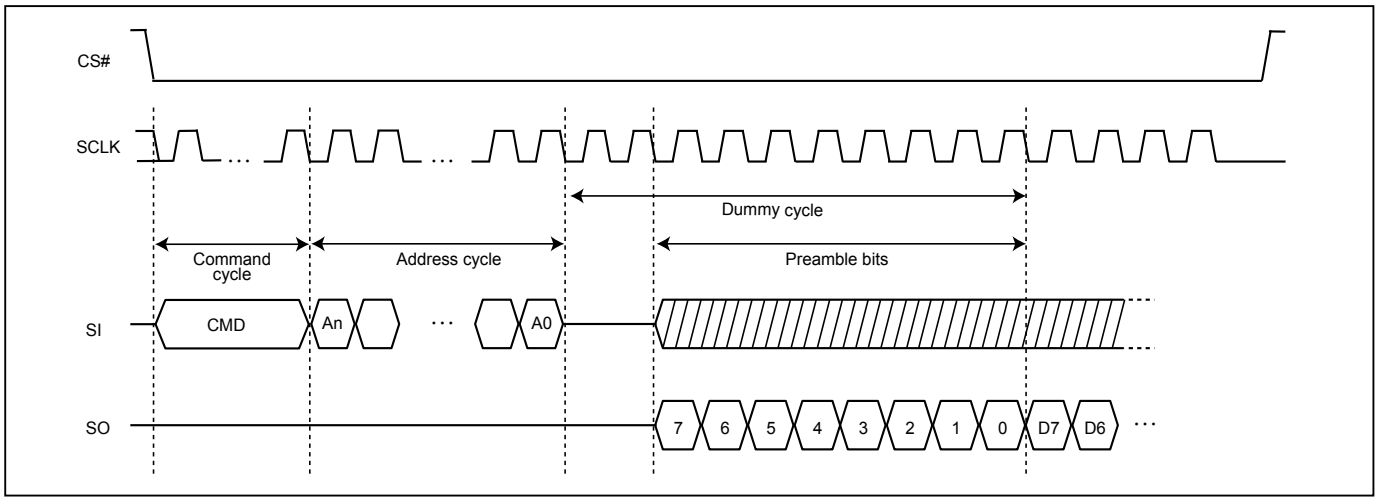


Figure 43. SDR 1I/O (8DC)

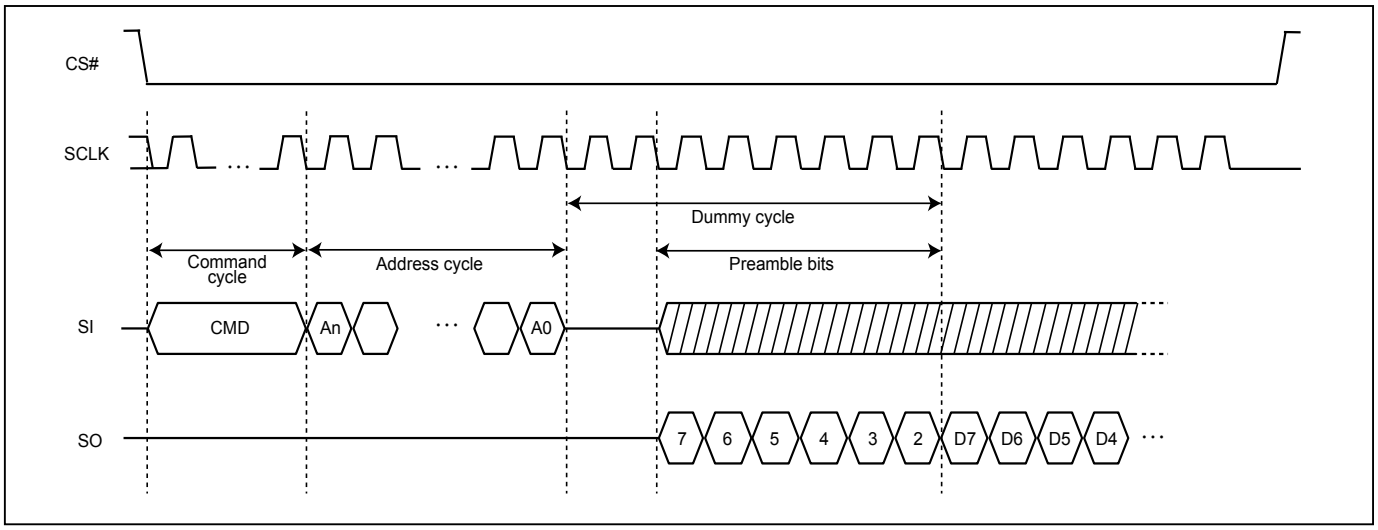


Figure 44. SDR 2I/O (10DC)

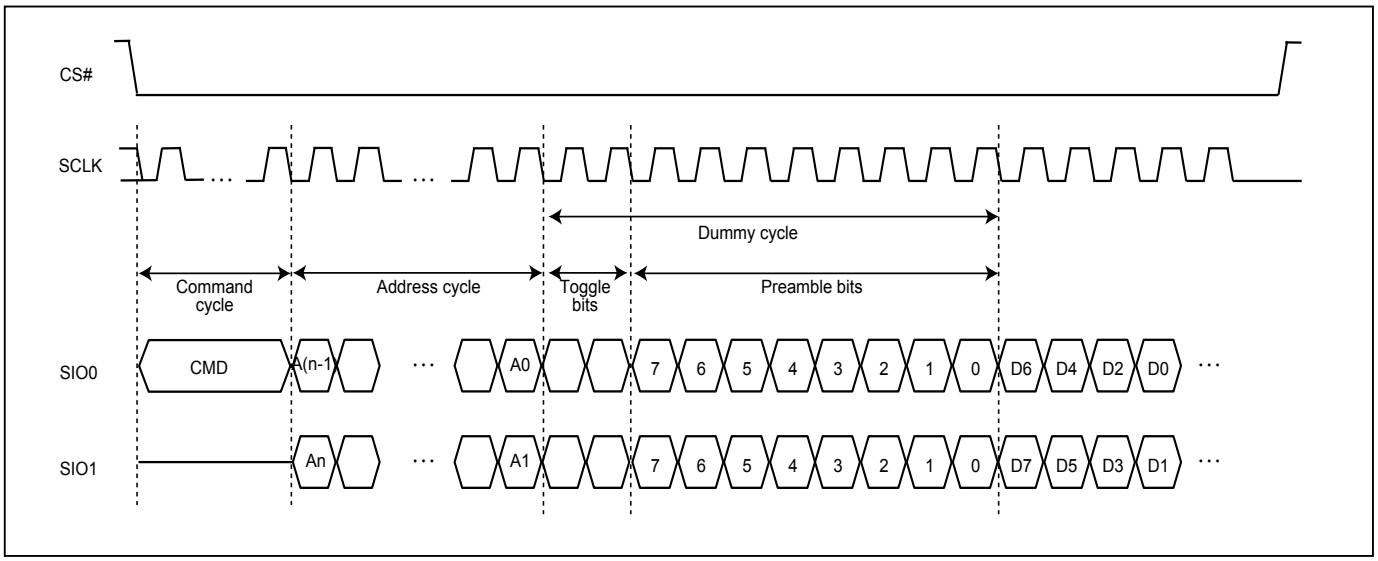


Figure 45. SDR 2I/O (8DC)

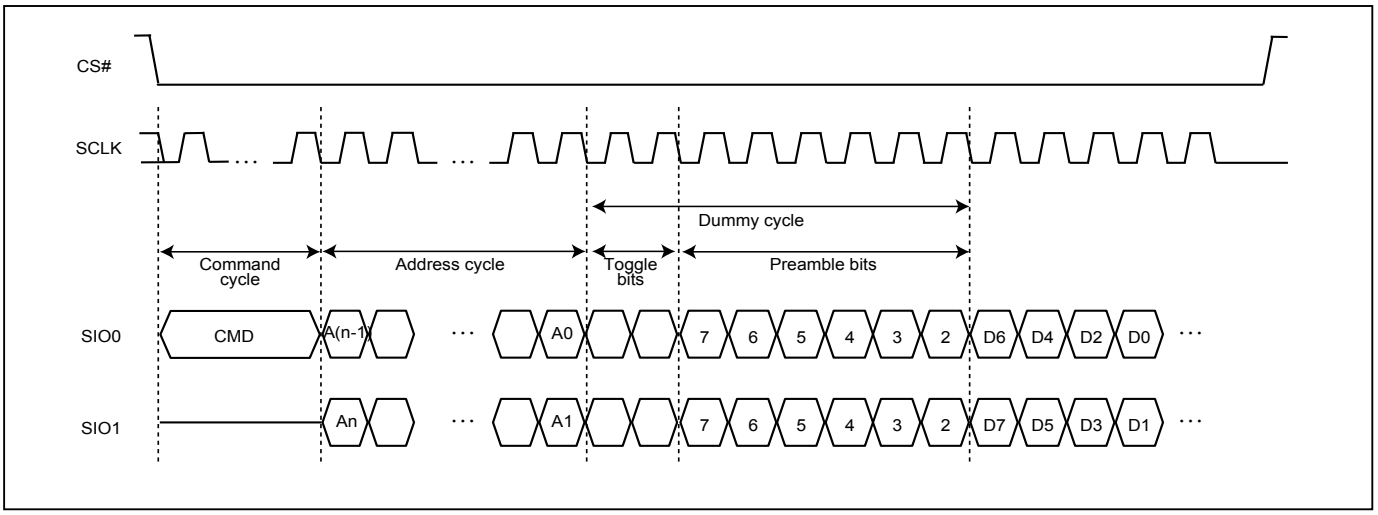


Figure 46. SDR 4I/O (10DC)

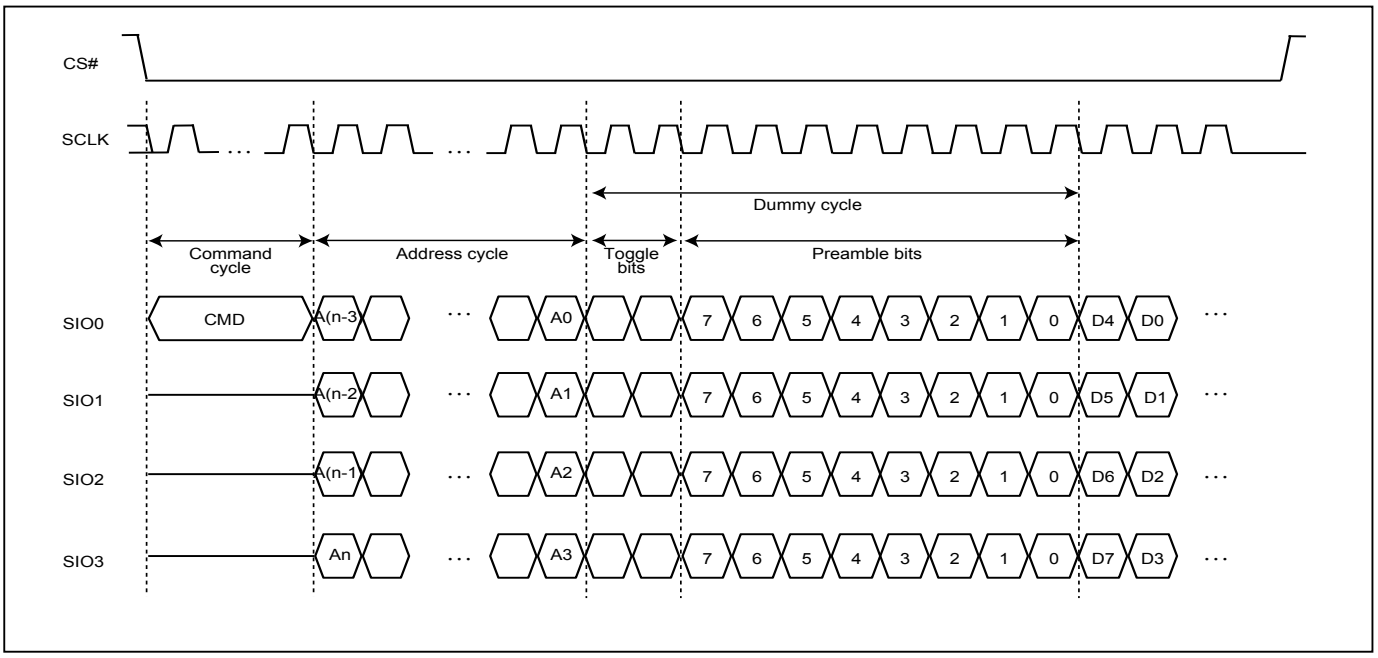


Figure 47. SDR 4I/O (8DC)

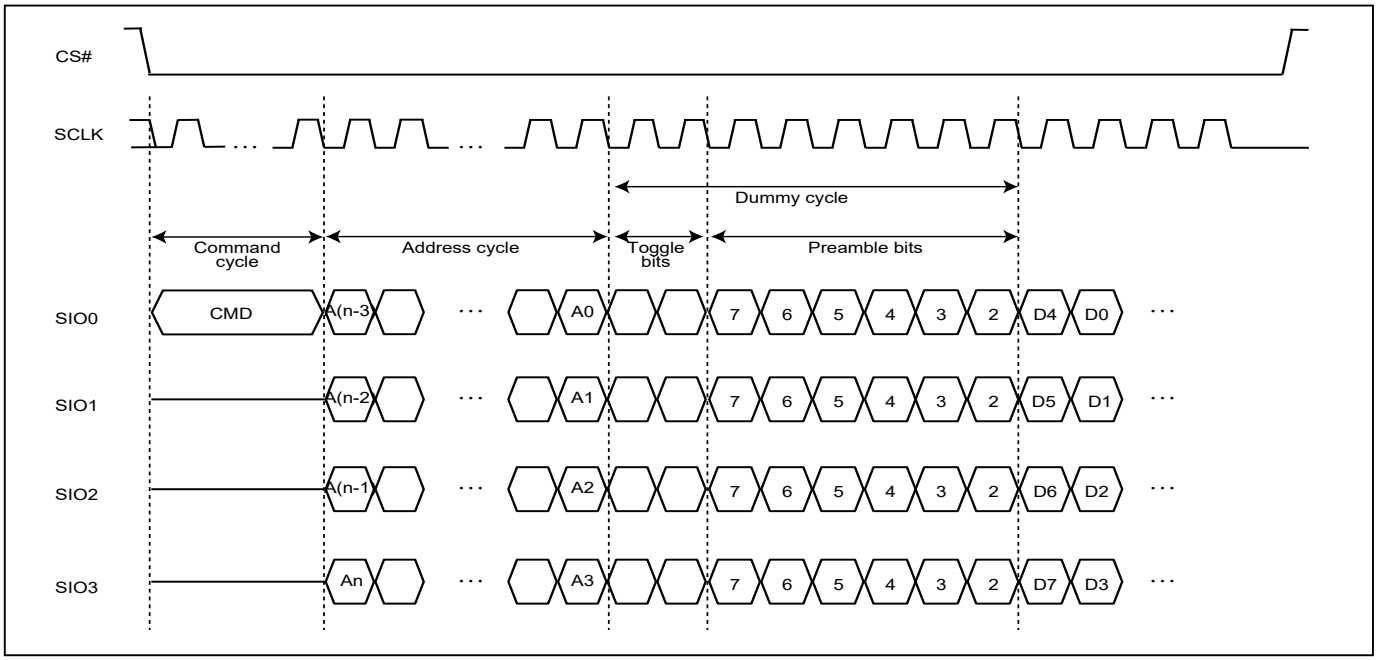
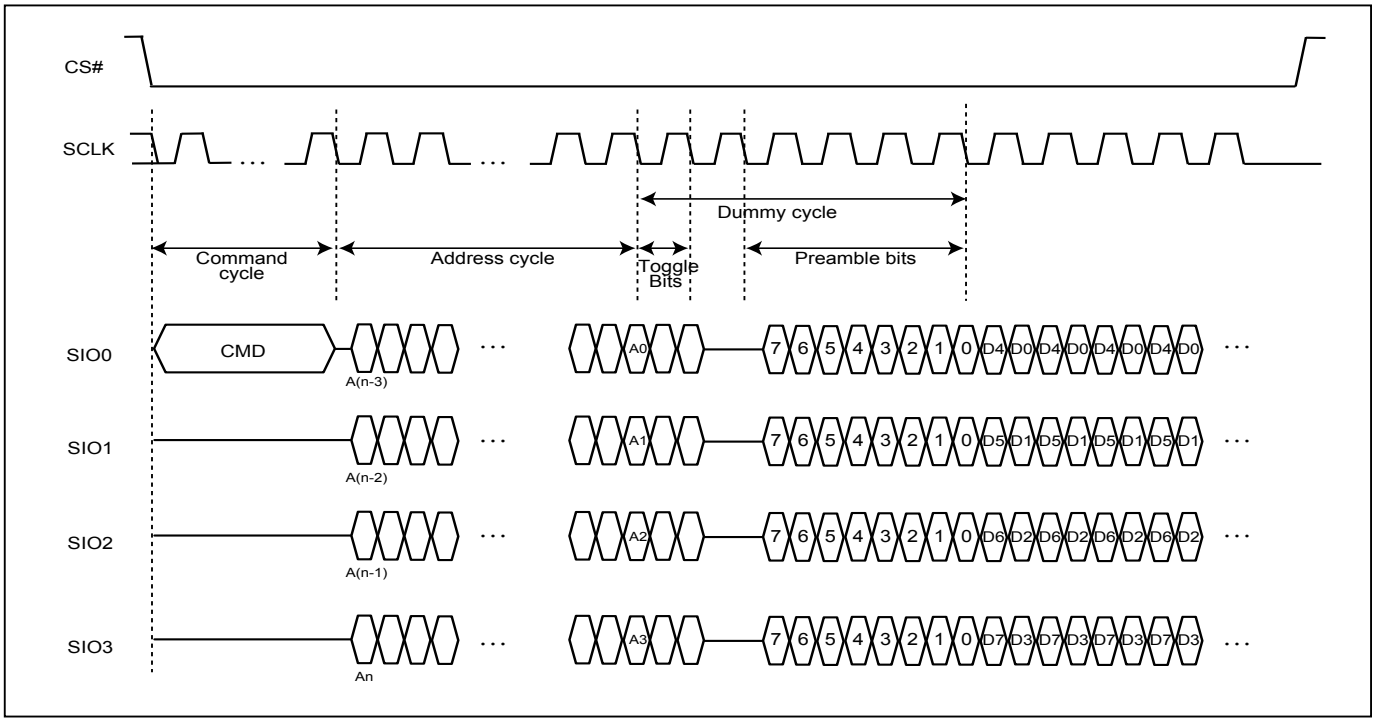


Figure 48. DTR4IO (6DC)



10-20. 4 Byte Address Command Set

The operation of 4-byte address command set was very similar to original 3-byte address command set. The only different is all the 4-byte command set request 4-byte address (A31-A0) followed by instruction code. The command set support 4-byte address including: READ4B, Fast_Read4B, DREAD4B, 2READ4B, QREAD4B, 4READ4B, 4DTRD4B, PP4B, 4PP4B, SE4B, BE32K4B, BE4B. Please note that it is not necessary to issue EN4B command before issuing any of 4-byte command set.

Figure 49. Read Data Bytes using 4 Byte Address Sequence (READ4B)

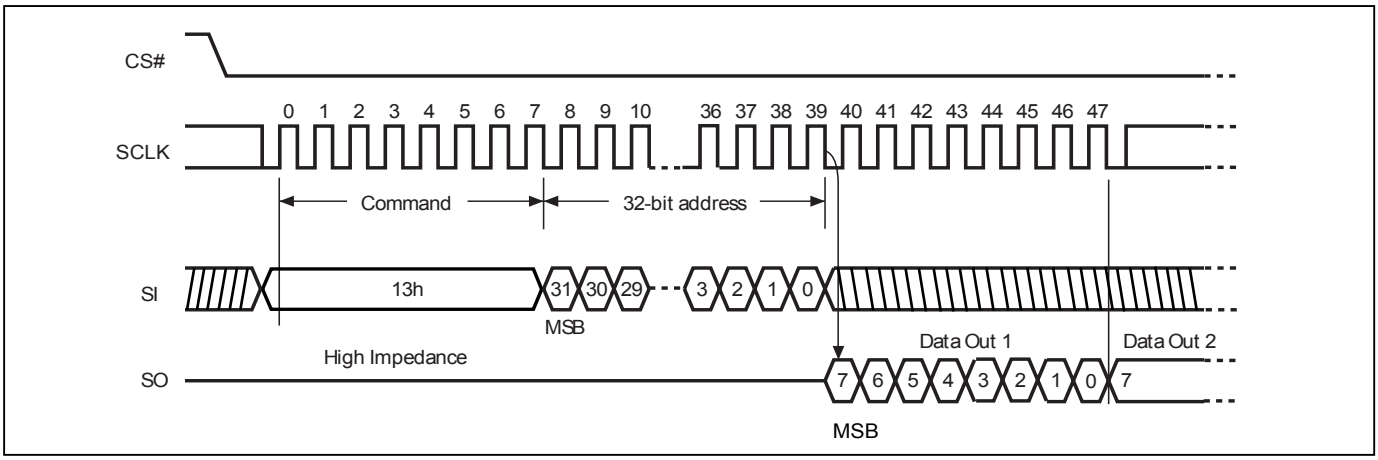
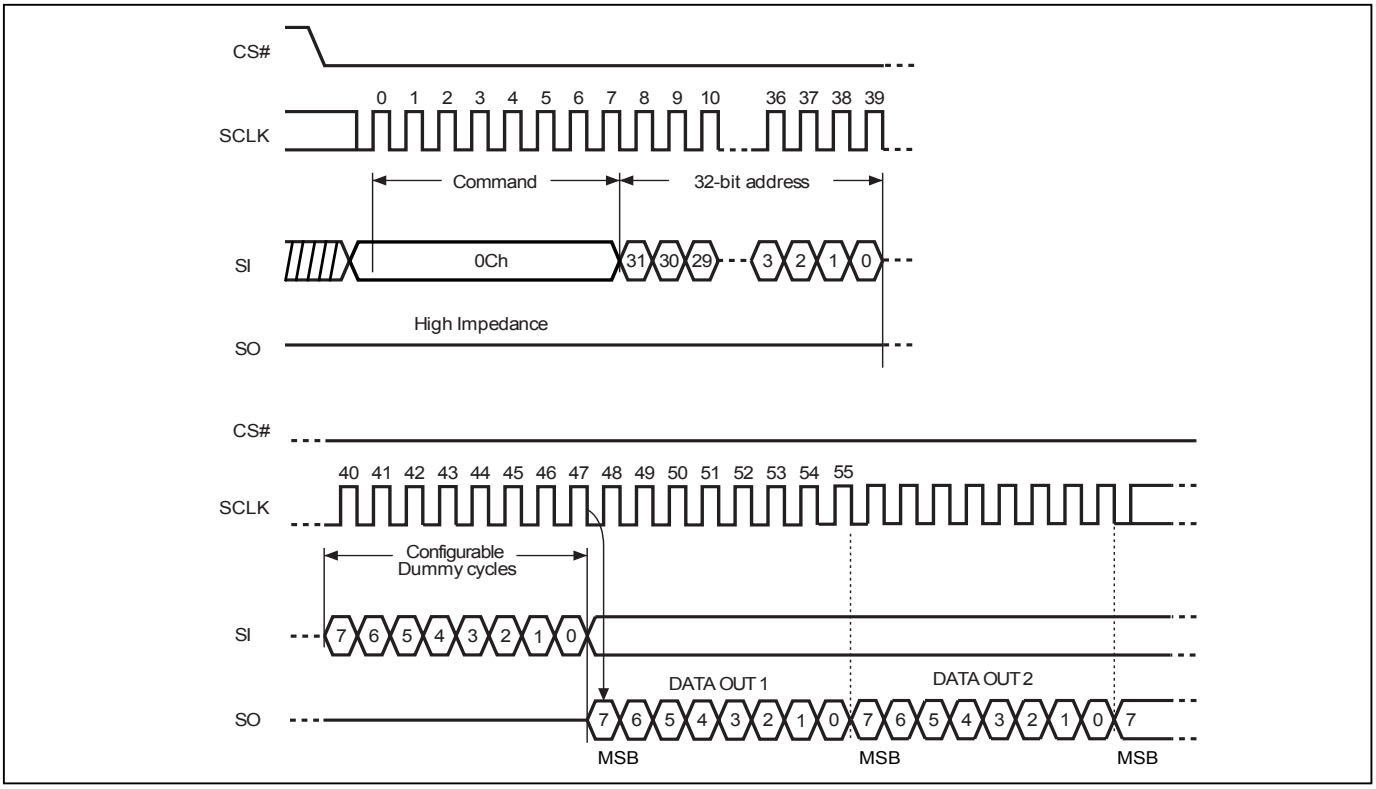
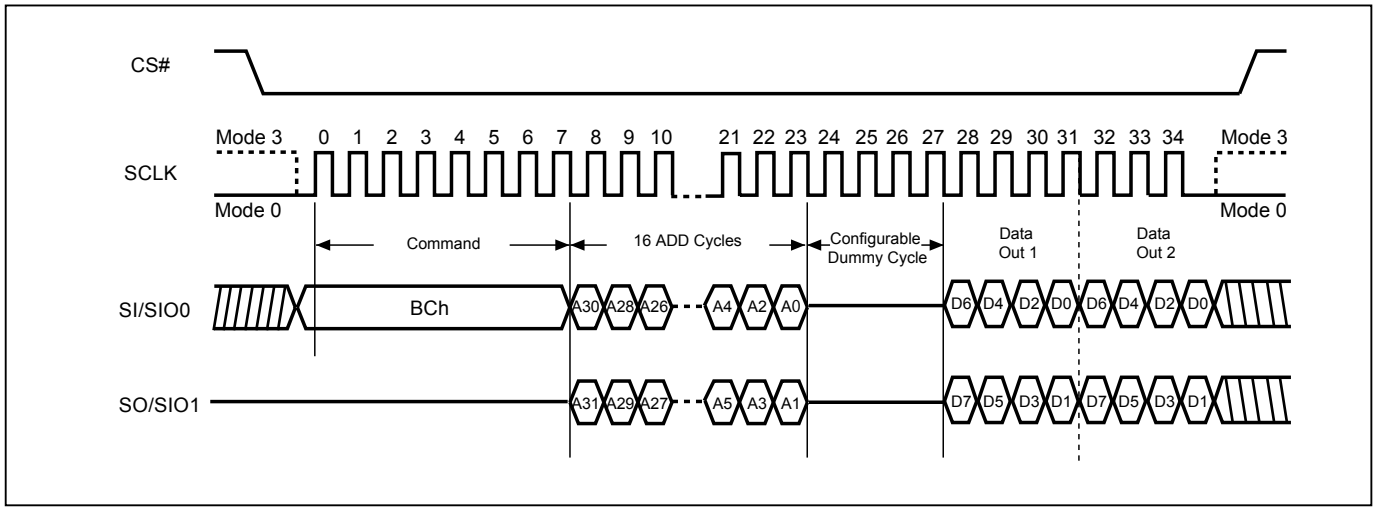


Figure 50. Read Data Bytes at Higher Speed using 4 Byte Address Sequence (FASTREAD4B)



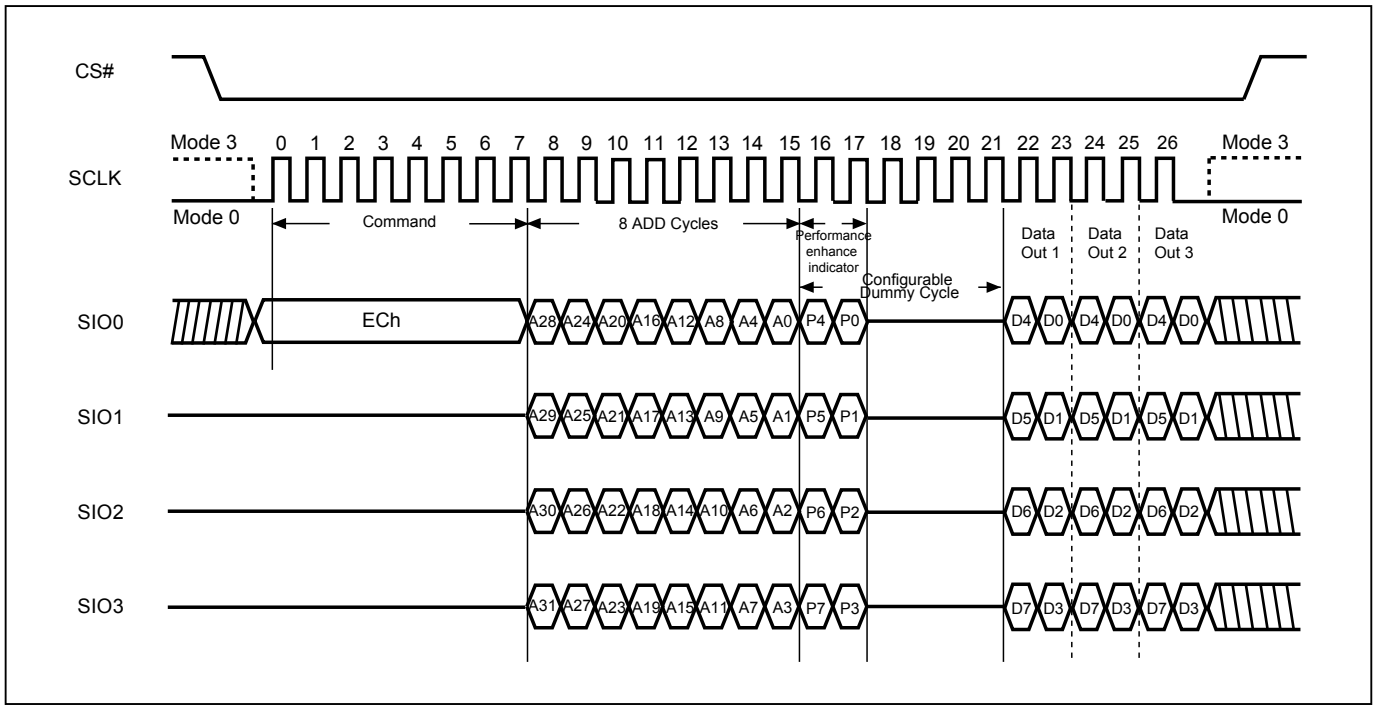
Note:
1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 51. 2 x I/O Fast Read using 4 Byte Address Sequence (2READ4B)



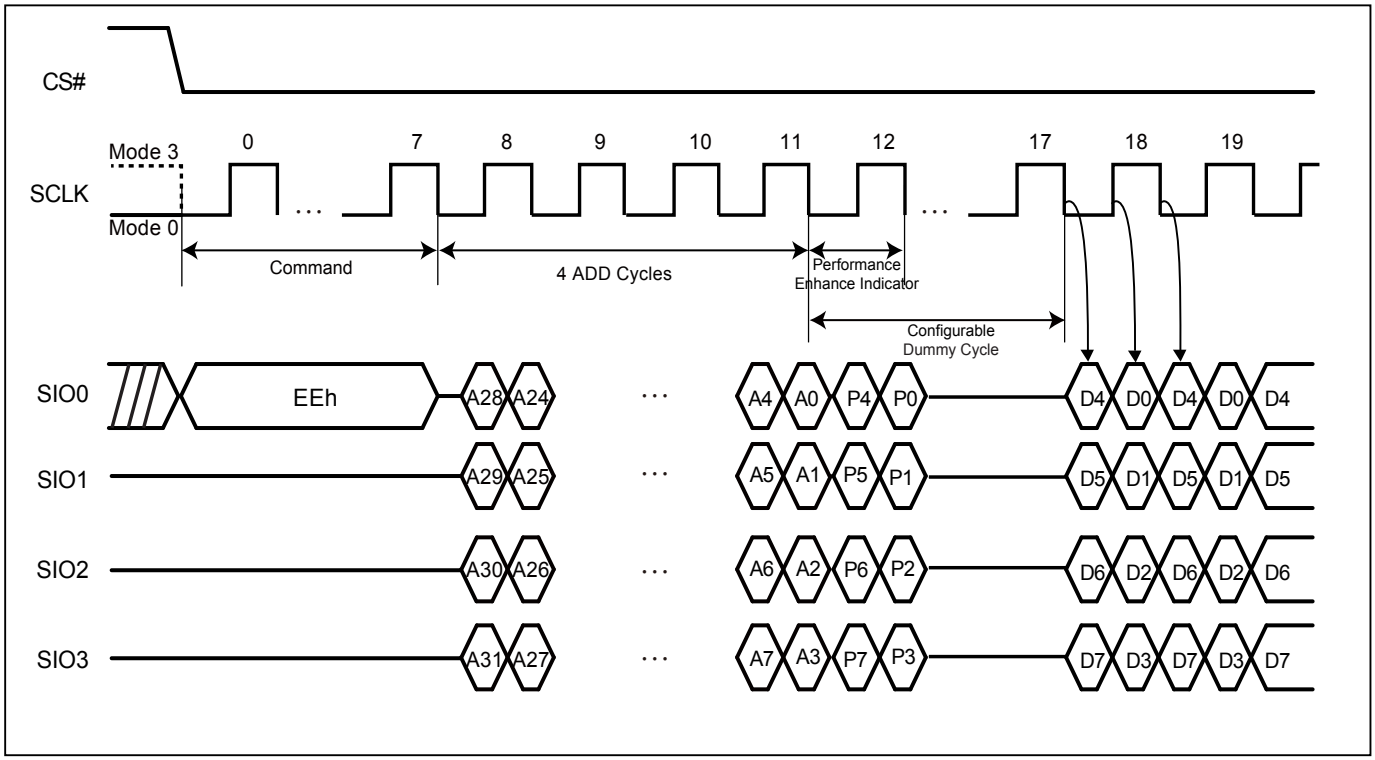
Note:
1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 52. 4 I/O Fast Read using 4 Byte Address sequence (4READ4B)



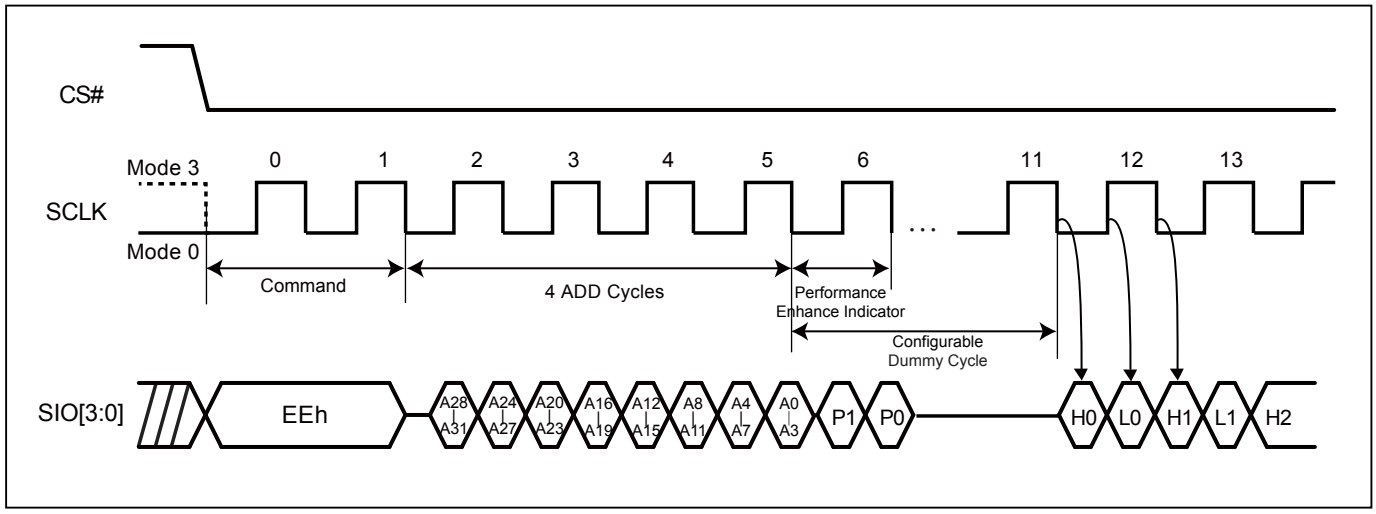
Note:
1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 53. Fast Quad I/O DT Read (4DTRD4B) Sequence (SPI Mode)



Note:
1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 54. Fast Quad I/O DT Read (4DTRD4B) Sequence (QPI Mode)



Note:
1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.

Figure 55. Sector Erase (SE4B) Sequence (SPI Mode)

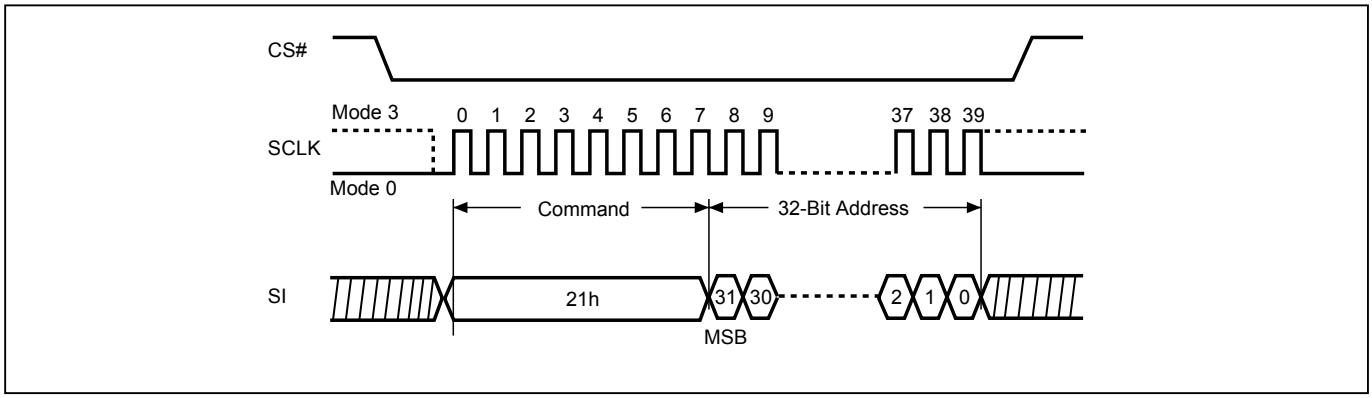


Figure 56. Block Erase 32KB (BE32K4B) Sequence (SPI Mode)

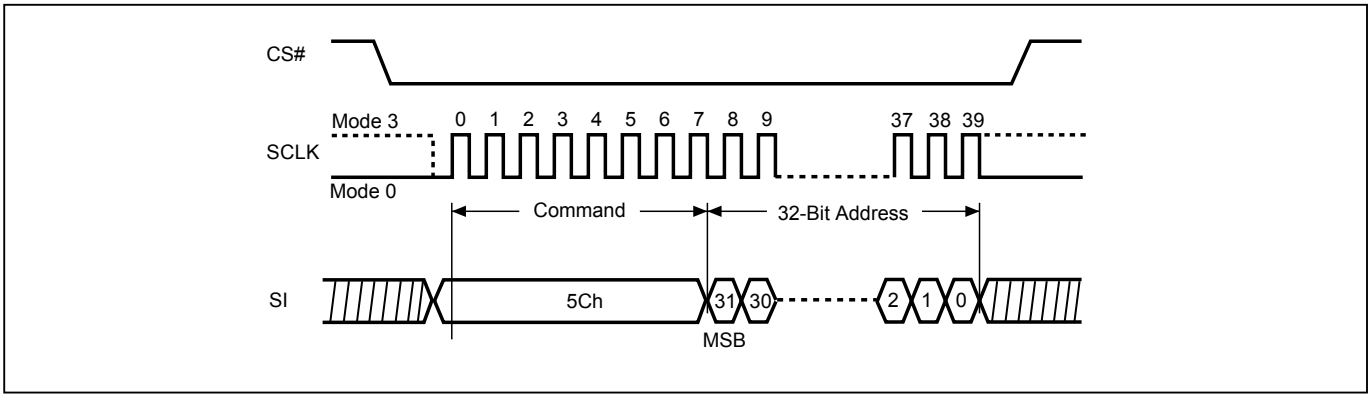


Figure 57. Block Erase (BE4B) Sequence (SPI Mode)

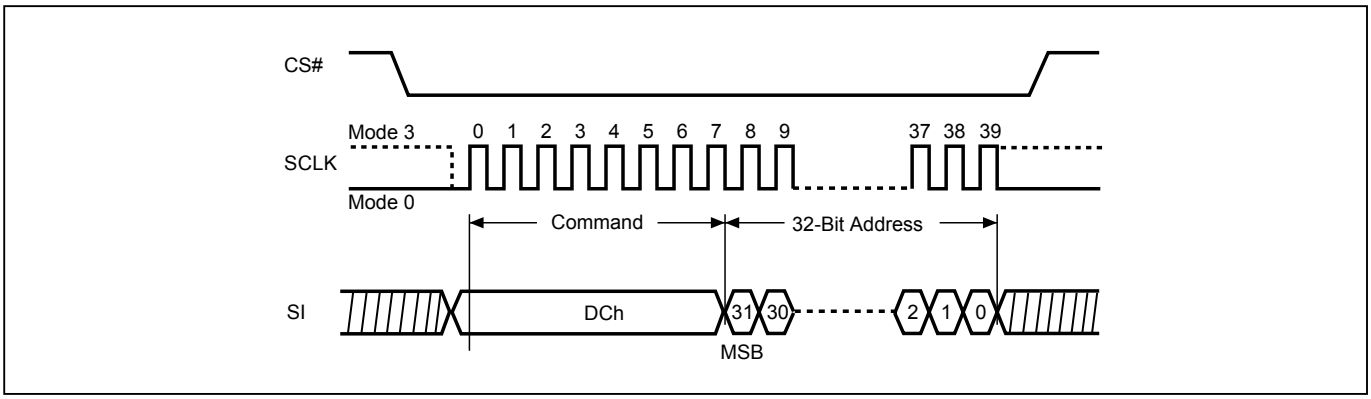


Figure 58. Page Program (PP4B) Sequence (SPI Mode)

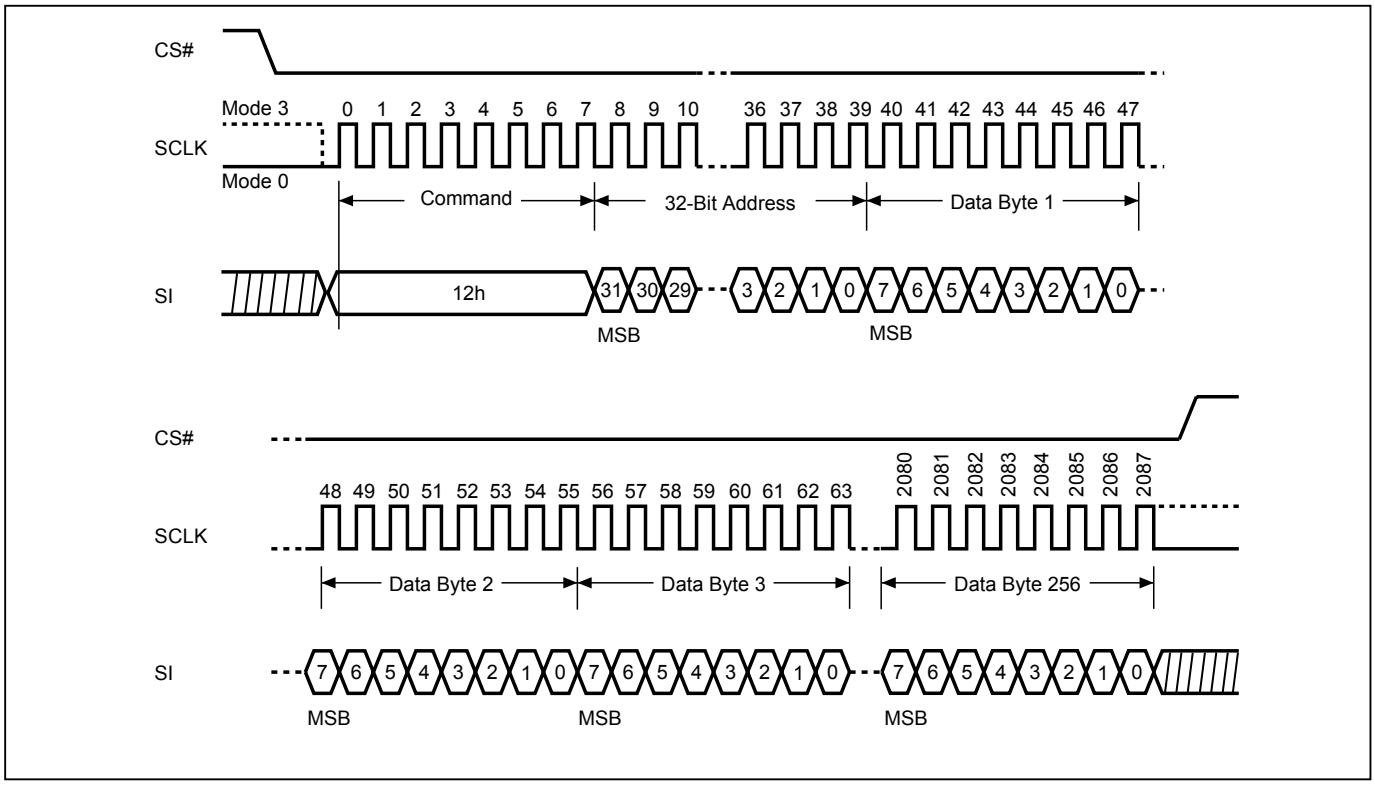
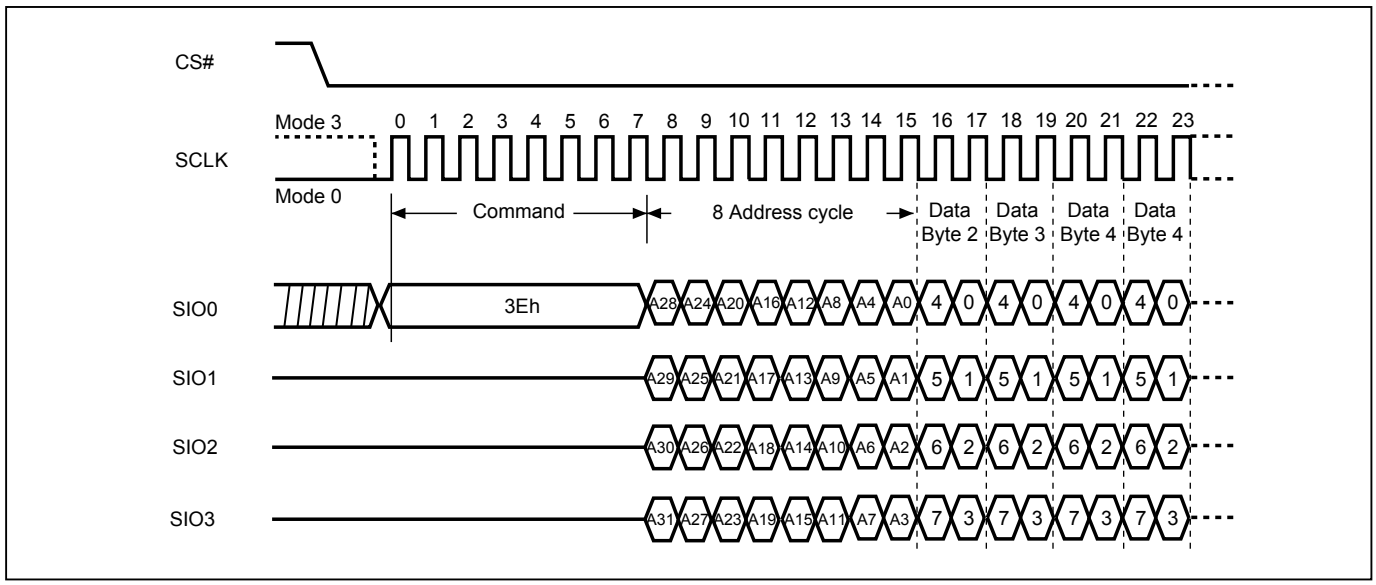


Figure 59. 4 x I/O Page Program (4PP4B) Sequence (SPI Mode only)



10-21. Performance Enhance Mode - XIP (execute-in-place)

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

Performance enhance mode is supported in both SPI and QPI mode.

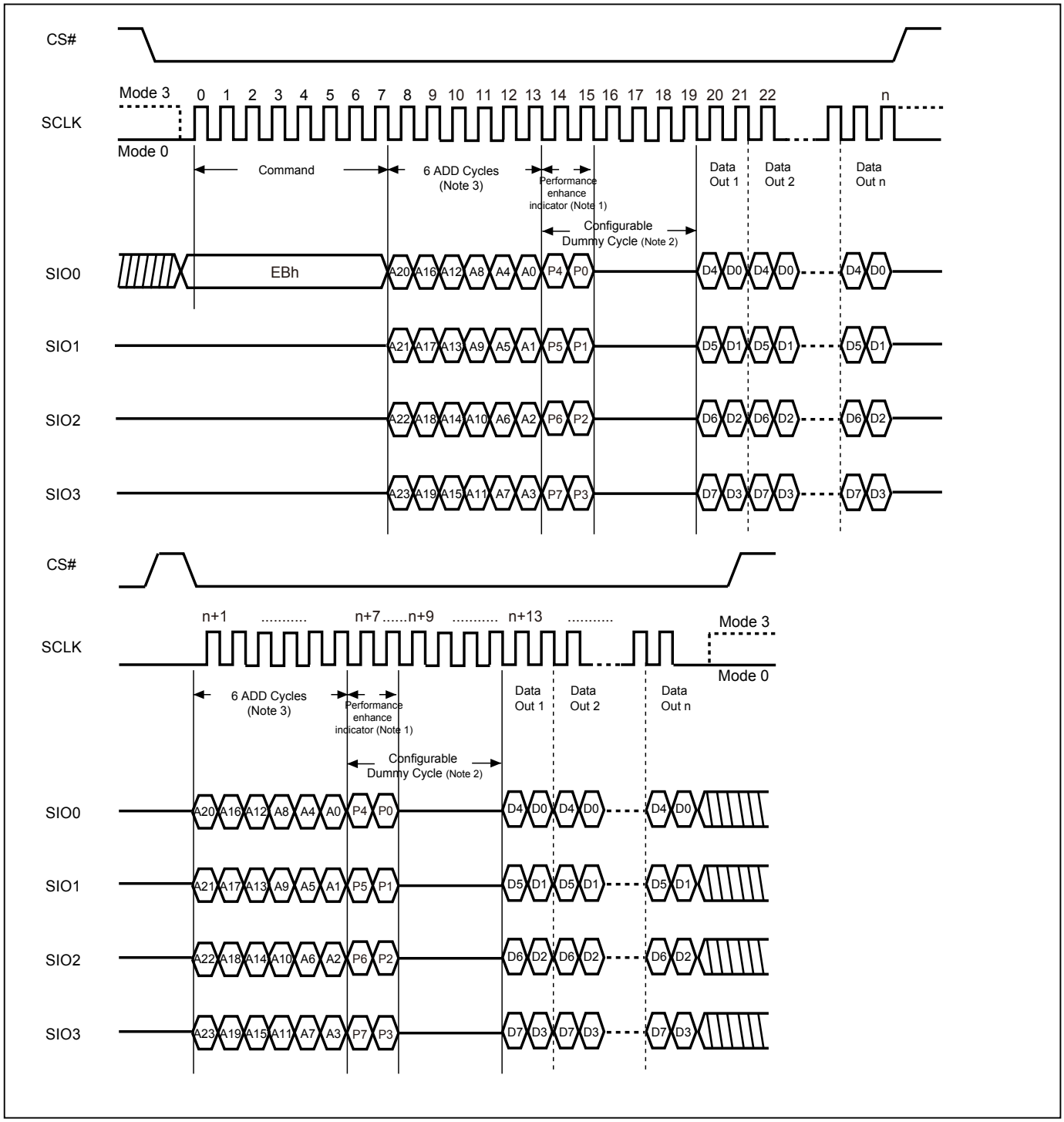
In QPI mode, “EBh” "ECh" "EDh" "EEh" and SPI “EBh” "ECh" "EDh" "EEh" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing ”FFh” data cycle can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes or 4-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles (Default) →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 3-bytes or 4-bytes random access address.

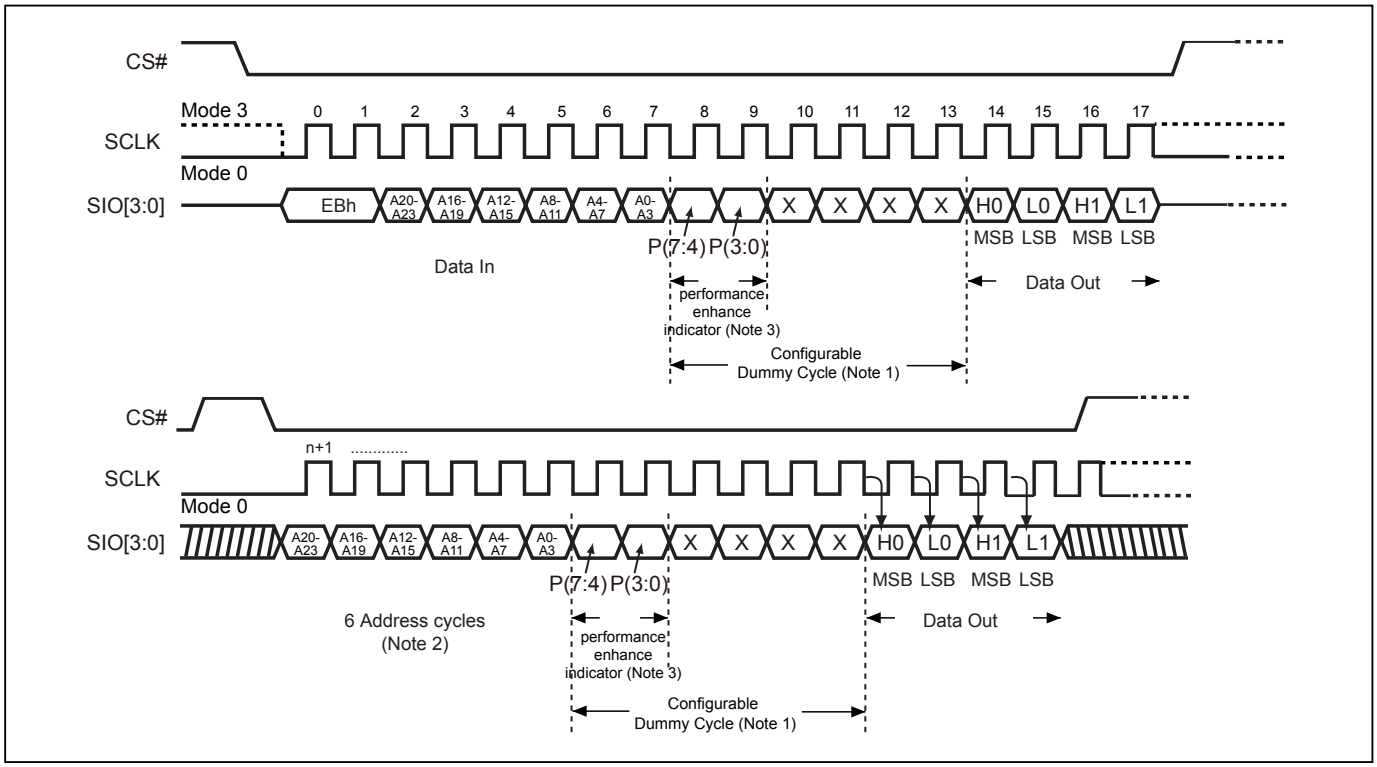
Figure 60. 4 x I/O Read Performance Enhance Mode Sequence (SPI Mode)



Notes:

1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.
2. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
3. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

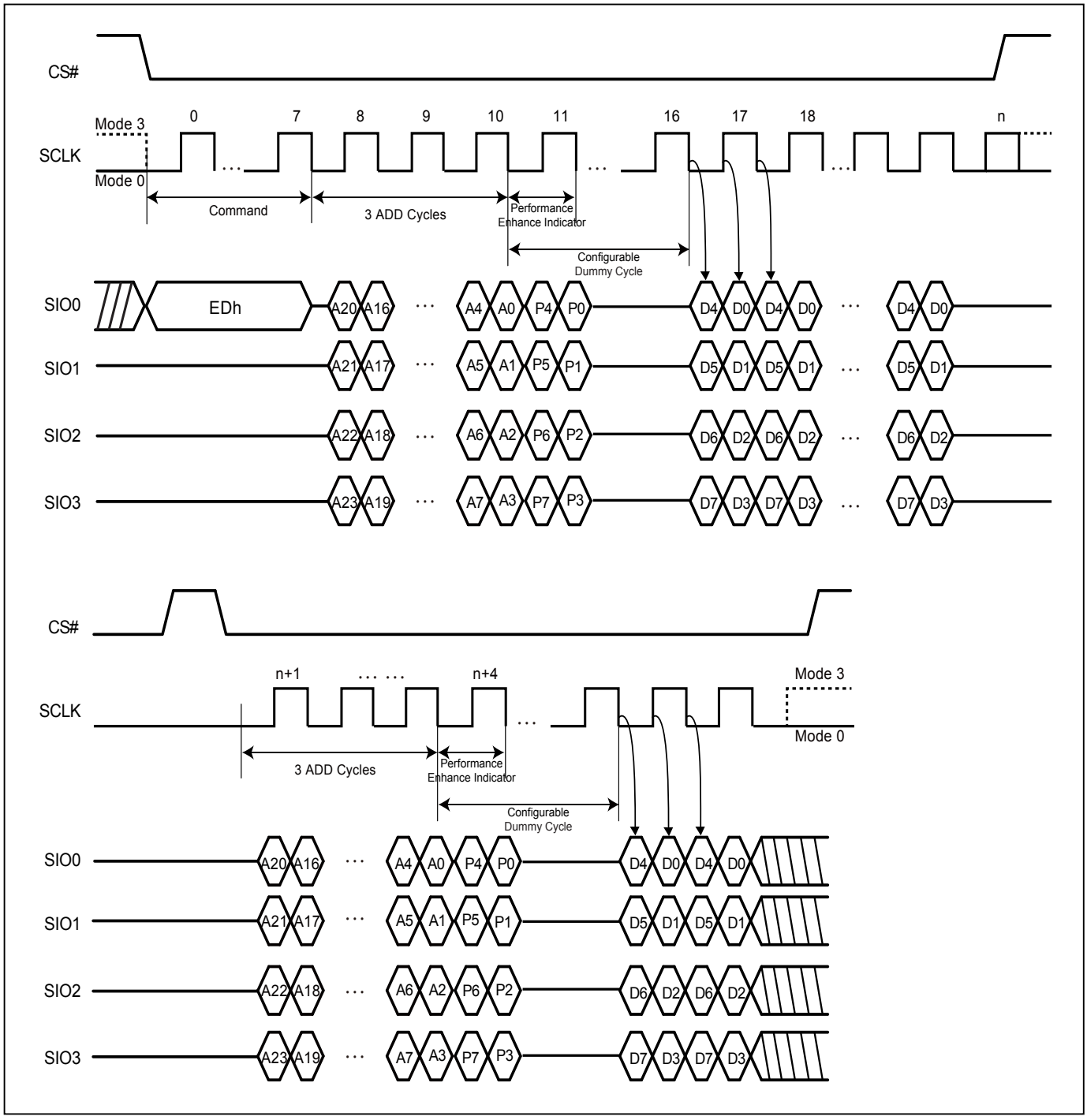
Figure 61. 4 x I/O Read Performance Enhance Mode Sequence (QPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
3. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.

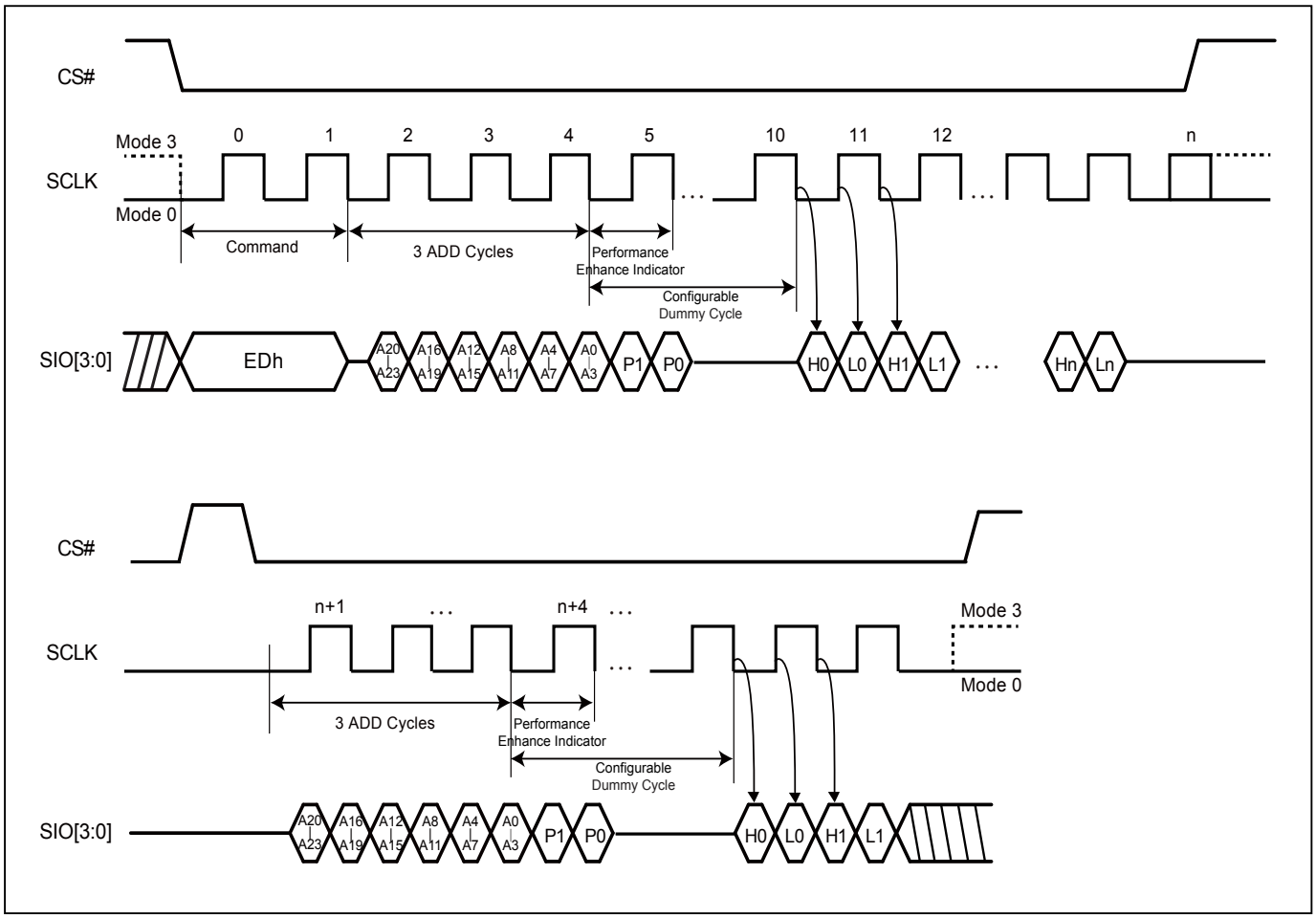
Figure 62. 4 x I/O DT Read Performance Enhance Mode Sequence (SPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
3. Reset the performance enhance mode, if P7=P3 or P6=P2 or P5=P1 or P4=P0, ex: AA, 00, FF.

Figure 63. 4 x I/O DT Read Performance Enhance Mode Sequence (QPI Mode)



Notes:

1. Configuration Dummy cycle numbers will be different depending on the bit6 & bit7 (DC0 & DC1) setting in configuration register.
2. Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.
3. Reset the performance enhance mode, if P1=P0, ex: AA, 00, FF.

10-22. Burst Read

To set the Burst length, following command operation is required to issue command: “C0h” in the first Byte (8-clocks), following 4 clocks defining wrap around enable with “0h” and disable with“1h”.

The next 4 clocks are to define wrap around depth. Their definitions are as the following table:

Data	Wrap Around	Wrap Depth
00h	Yes	8-byte
01h	Yes	16-byte
02h	Yes	32-byte
03h	Yes	64-byte
1xh	No	X

The wrap around unit is defined with the 8/16/32/64Byte, with random initial address. It is defined as “wrap-around mode disable” for the default state of the device. To exit wrap around, it is required to issue another “C0h” command in which data=‘1xh”. Otherwise, wrap around status will be retained until power down or reset command. To change wrap around depth, it is requried to issue another “C0h” command in which data=“0xh”. QPI “EBh” "ECh" and SPI “EBh” "ECh" support wrap around feature after wrap around is enabled. Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 64. SPI Mode

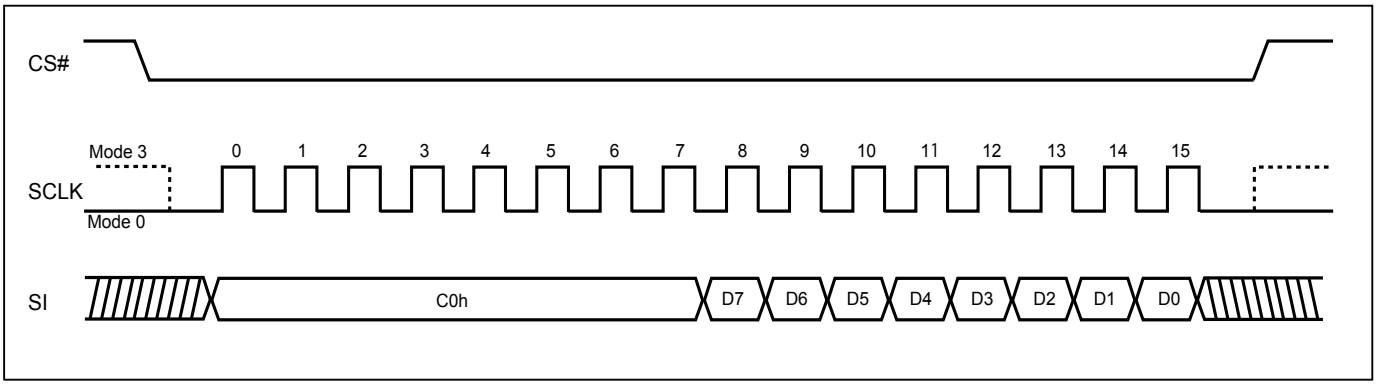
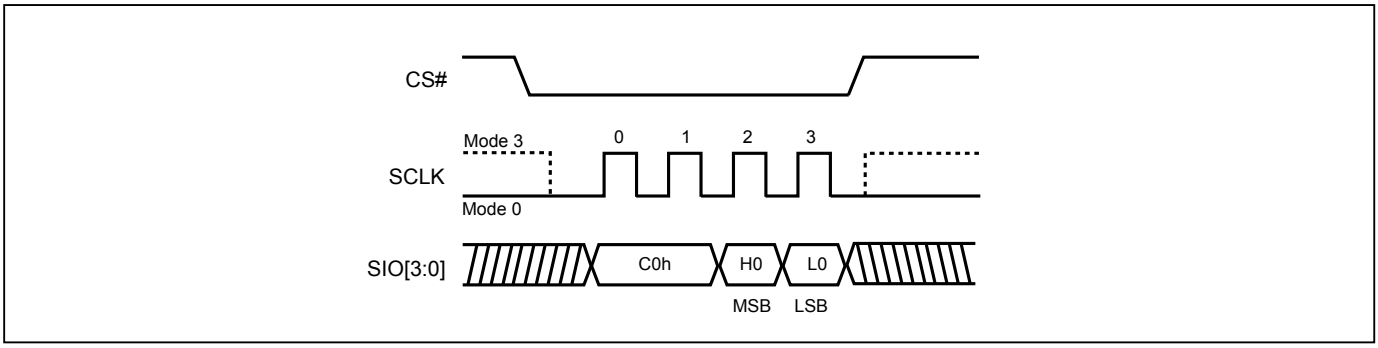


Figure 65. QPI Mode



Note: MSB=Most Significant Bit
LSB=Least Significant Bit

10-23. Fast Boot

The Fast Boot Feature provides the ability to automatically execute read operation after power on cycle or reset without any read instruction.

A Fast Boot Register is provided on this device. It can enable the Fast Boot function and also define the number of delay cycles and start address (where boot code being transferred). Instruction WRFBR (write fast boot register) and ESFBR (erase fast boot register) can be used for the status configuration or alternation of the Fast Boot Register bit. RDFBR (read fast boot register) can be used to verify the program state of the Fast Boot Register. The default number of delay cycles is 13 cycles, and there is a 16bytes boundary address for the start of boot code access.

When CS# starts to go low, data begins to output from default address after the delay cycles (default as 13 cycles). After CS# returns to go high, the device will go back to standard SPI mode and user can start to input command. In the fast boot data out process from CS# goes low to CS# goes high, a minimum of one byte must be output.

Once Fast Boot feature has been enabled, the device will automatically start a read operation after power on cycle, reset command, or hardware reset operation.

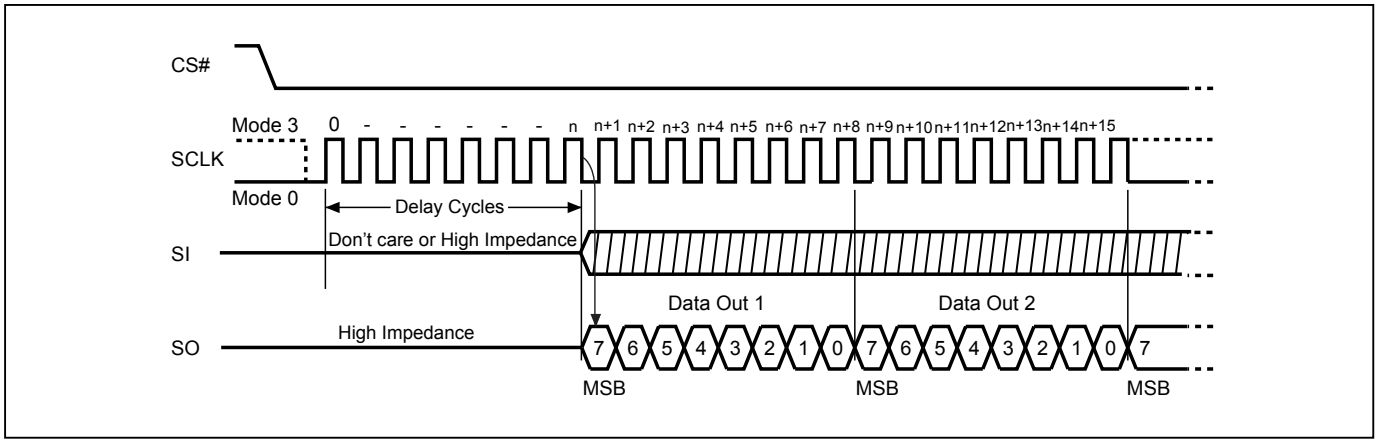
The fast Boot feature can support Single I/O and Quad I/O interface. If the QE bit of Status Register is “0”, the data is output by Single I/O interface. If the QE bit of Status Register is set to “1”, the data is output by Quad I/O interface.

Fast Boot Register (FBR)

Bits	Description	Bit Status	Default State	Type
31 to 4	FBSA (FastBoot Start Address)	16 bytes boundary address for the start of boot code access.	FFFFFFF	Non-Volatile
3	x		1	Non-Volatile
2 to 1	FBSD (FastBoot Start Delay Cycle)	00: 7 delay cycles 01: 9 delay cycles 10: 11 delay cycles 11: 13 delay cycles	11	Non-Volatile
0	FBE (FastBoot Enable)	0=FastBoot is enabled. 1=FastBoot is not enabled.	1	Non-Volatile

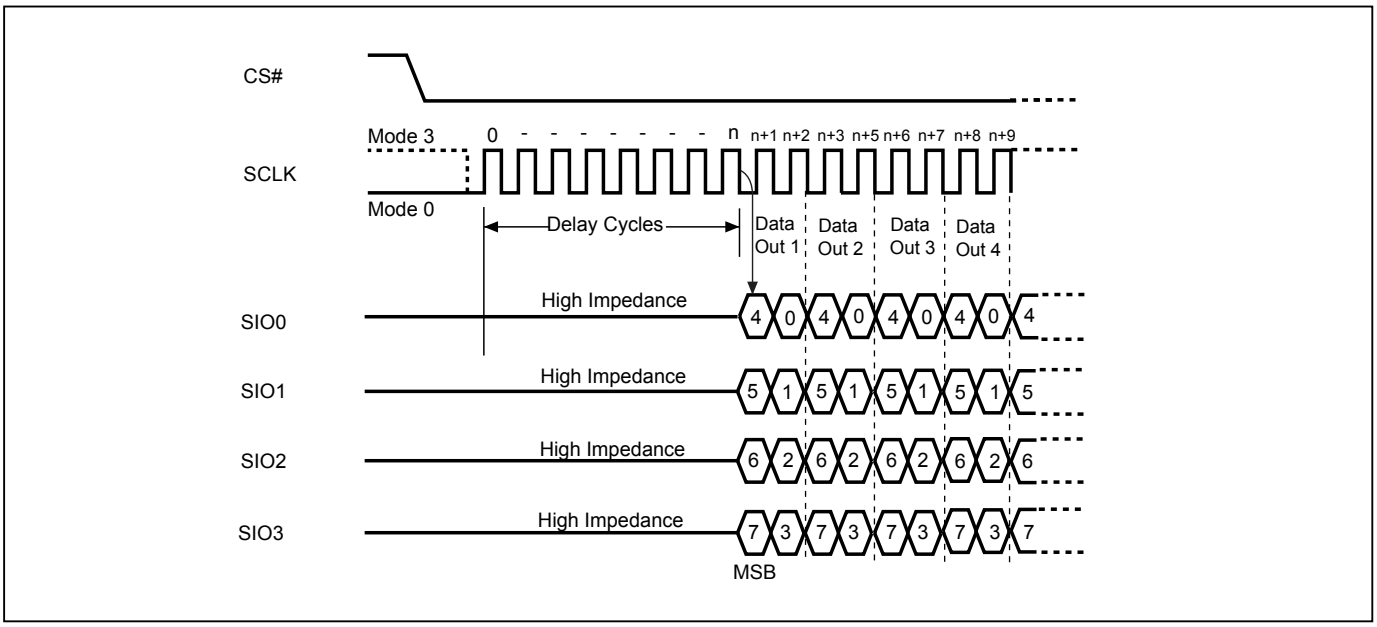
Note: If FBSD = 11, the maximum clock frequency is 133 MHz
If FBSD = 10, the maximum clock frequency is 104 MHz
If FBSD = 01, the maximum clock frequency is 84 MHz
If FBSD = 00, the maximum clock frequency is 70 MHz

Figure 66. Fast Boot Sequence (QE=0)



Note: If FBSD = 11, delay cycles is 13 and n is 12.
If FBSD = 10, delay cycles is 11 and n is 10.
If FBSD = 01, delay cycles is 9 and n is 8.
If FBSD = 00, delay cycles is 7 and n is 6.

Figure 67. Fast Boot Sequence (QE=1)



Note: If FBSD = 11, delay cycles is 13 and n is 12.
If FBSD = 10, delay cycles is 11 and n is 10.
If FBSD = 01, delay cycles is 9 and n is 8.
If FBSD = 00, delay cycles is 7 and n is 6.

Figure 68. Read Fast Boot Register (RDFBR) Sequence

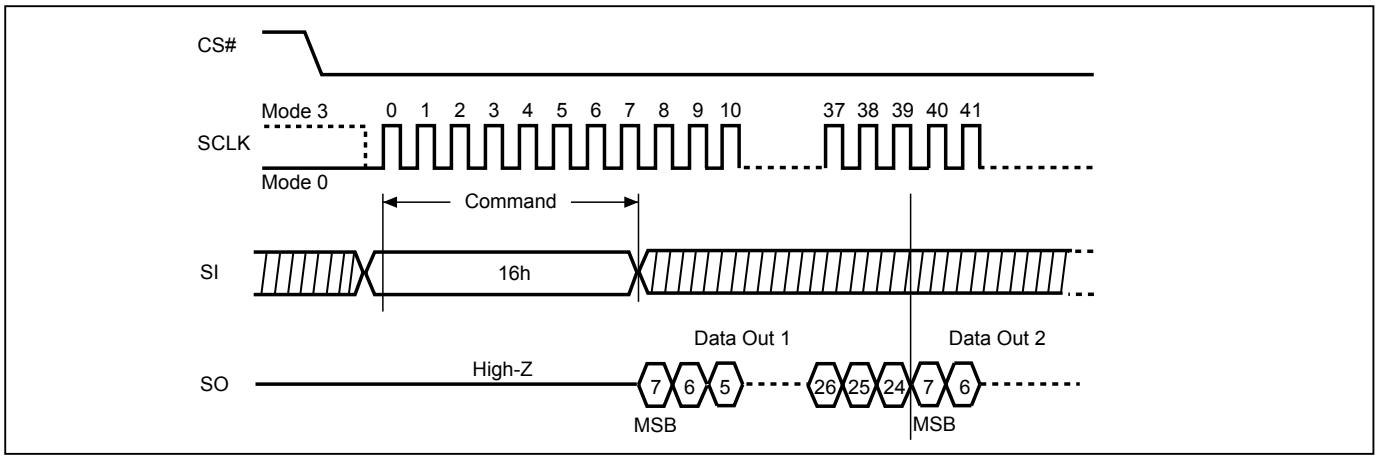


Figure 69. Write Fast Boot Register (WRFBR) Sequence

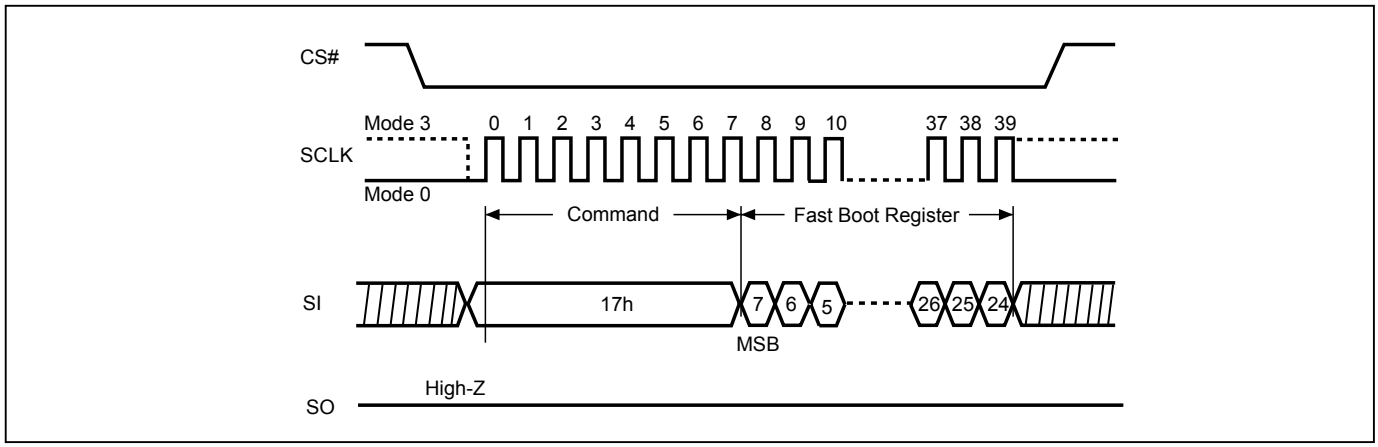
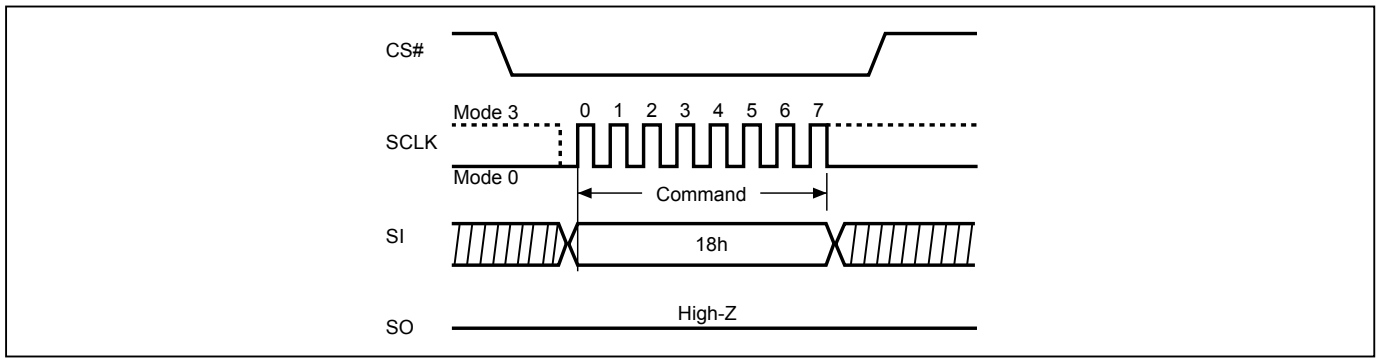


Figure 70. Erase Fast Boot Register (ESFBR) Sequence



10-24. Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. Address bits [Am-A12] (Am is the most significant address) select the sector address.

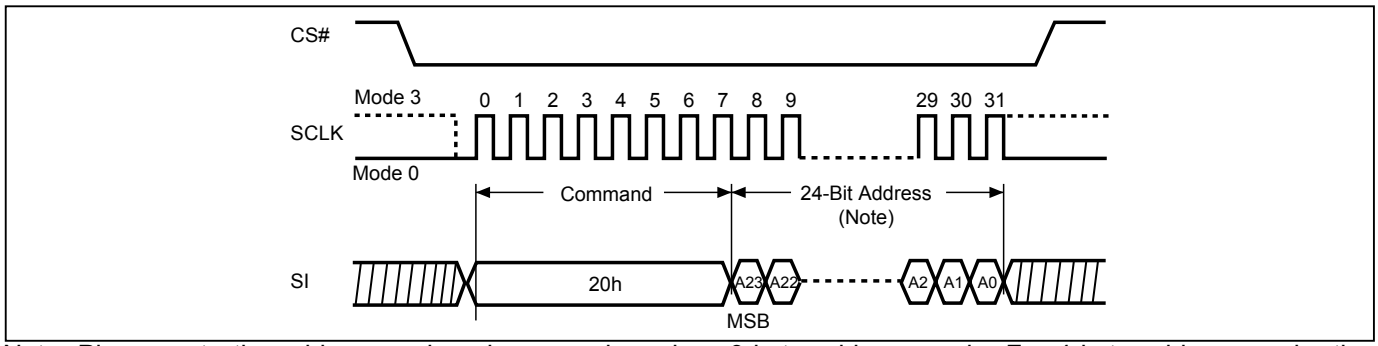
To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

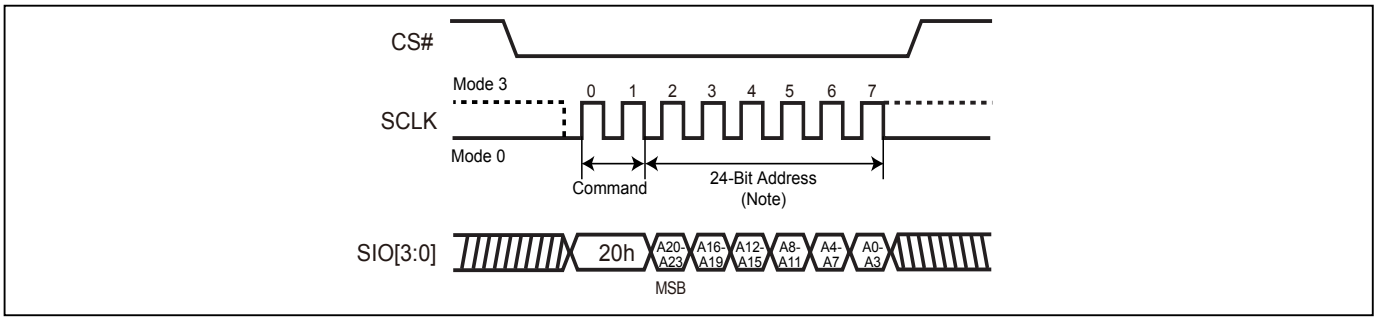
The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Sector Erase (SE) instruction will not be executed on the block.

Figure 71. Sector Erase (SE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 72. Sector Erase (SE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-25. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

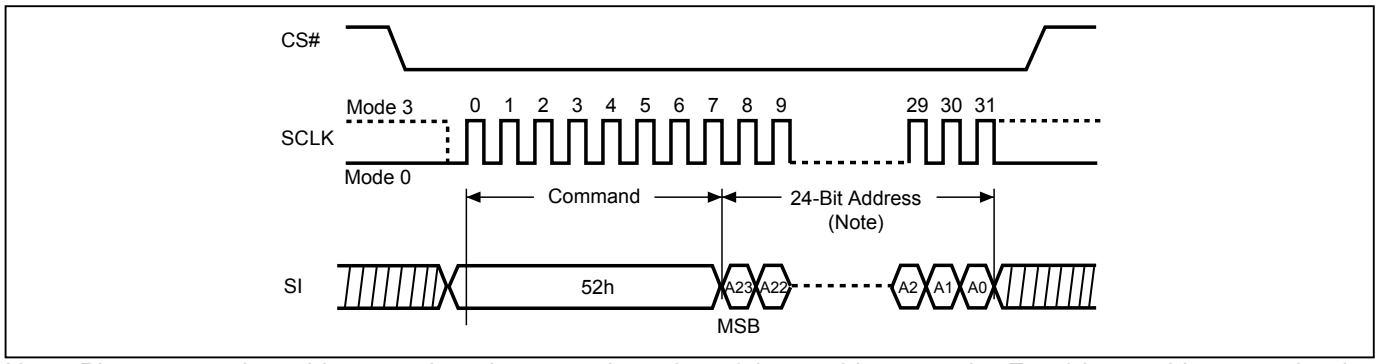
Address bits [Am-A15] (Am is the most significant address) select the 32KB block address. The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte or 4-byte address on SI→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

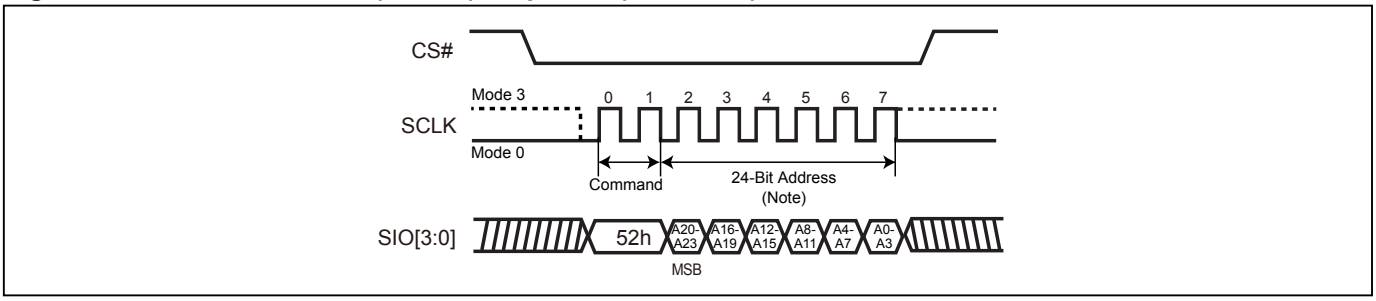
The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Block Erase (BE32K) instruction will not be executed on the block.

Figure 73. Block Erase 32KB (BE32K) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 74. Block Erase 32KB (BE32K) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-26. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"5. MEMORY ORGANIZATION"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

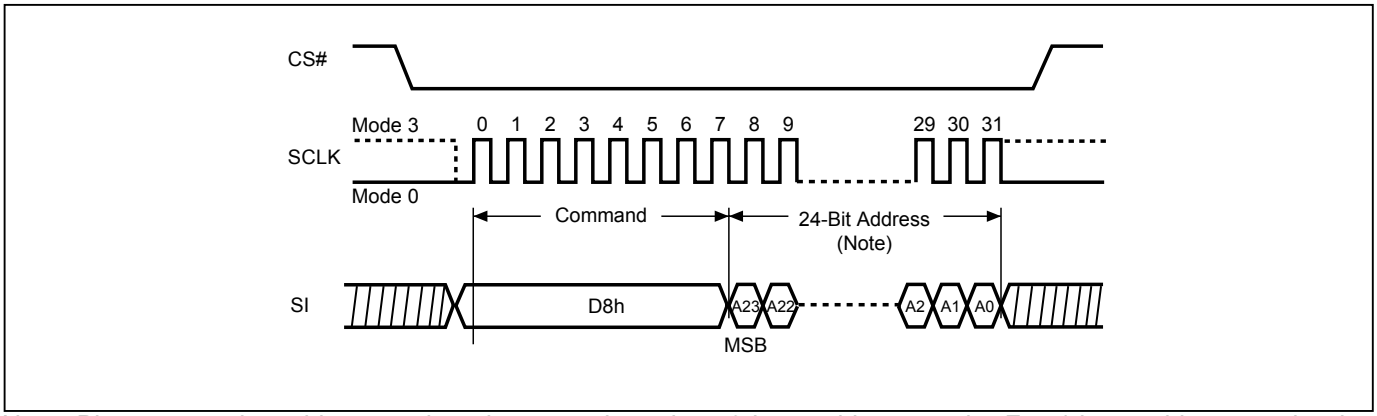
The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte or 4-byte address on SI→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

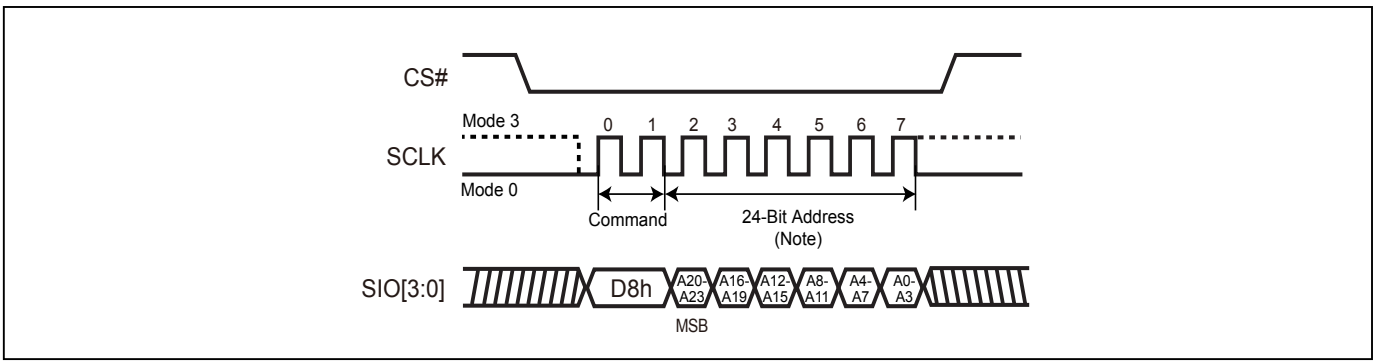
The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Block Erase (BE) instruction will not be executed on the block.

Figure 75. Block Erase (BE) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 76. Block Erase (BE) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-27. Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode" (WPSEL=0). The Chip Erase (CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Advances Sector Protect Mode" (WPSEL=1). The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

Figure 77. Chip Erase (CE) Sequence (SPI Mode)

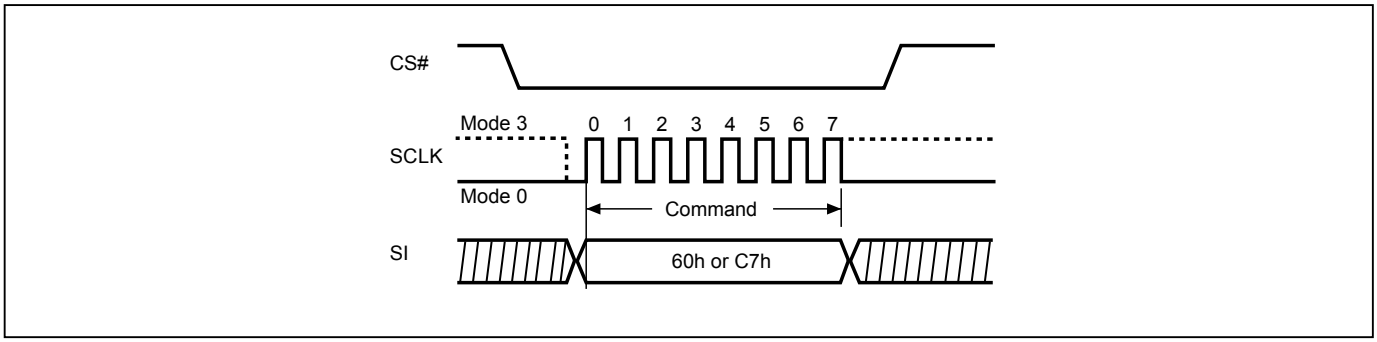
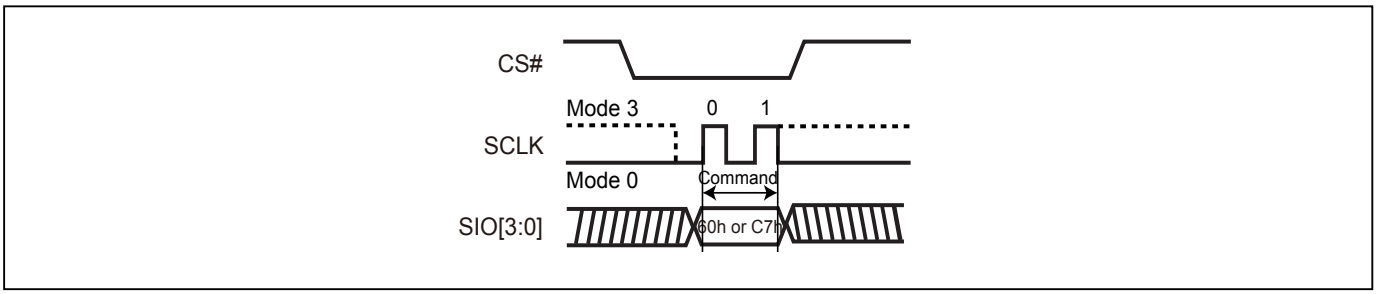


Figure 78. Chip Erase (CE) Sequence (QPI Mode)



10-28. Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) must be set to 0. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. Partial program or double program are not allowed.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

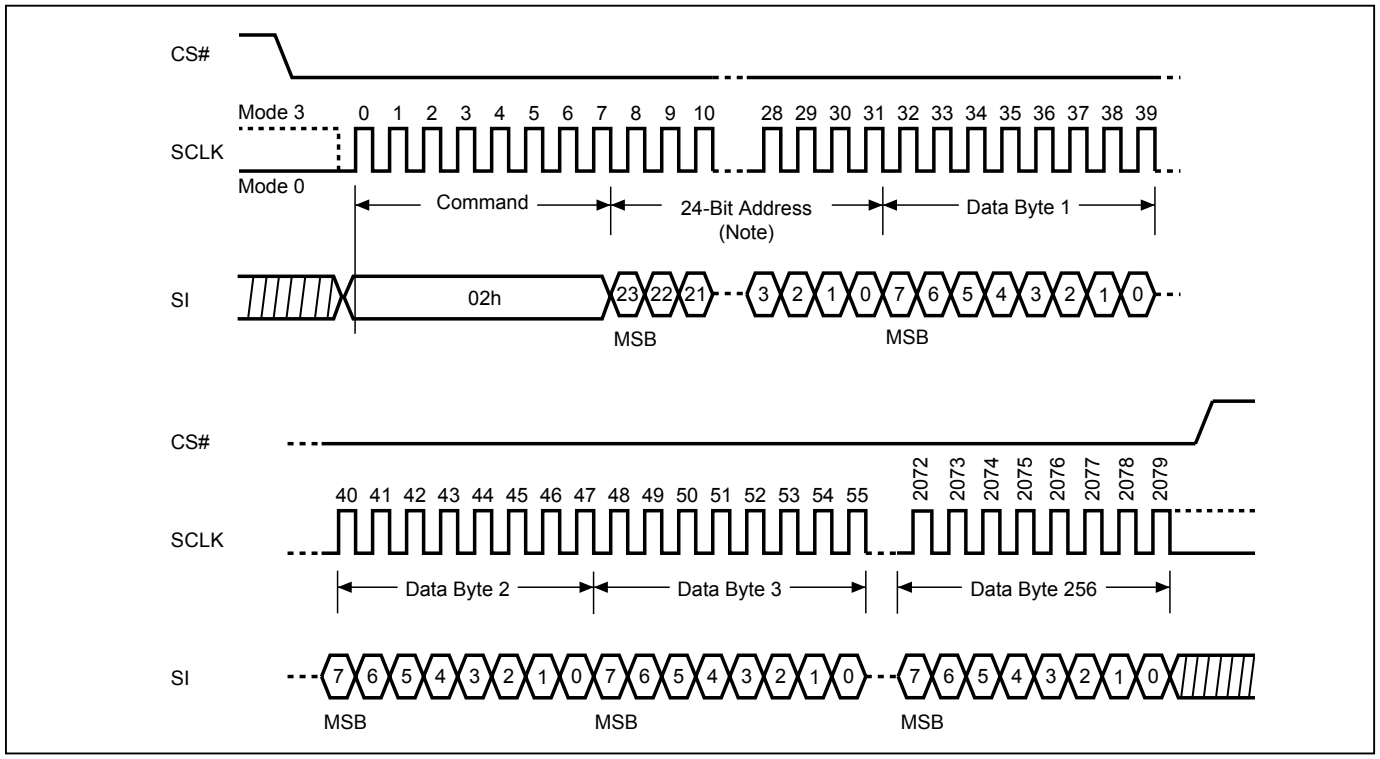
The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte or 4-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Page Program (PP) instruction will not be executed.

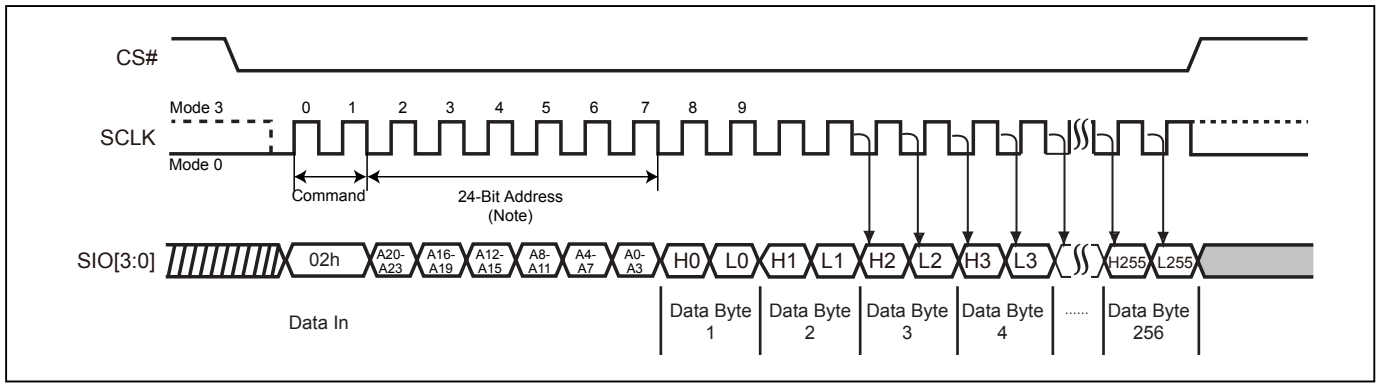
Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Figure 79. Page Program (PP) Sequence (SPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

Figure 80. Page Program (PP) Sequence (QPI Mode)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-29. 4 x I/O Page Program (4PP)

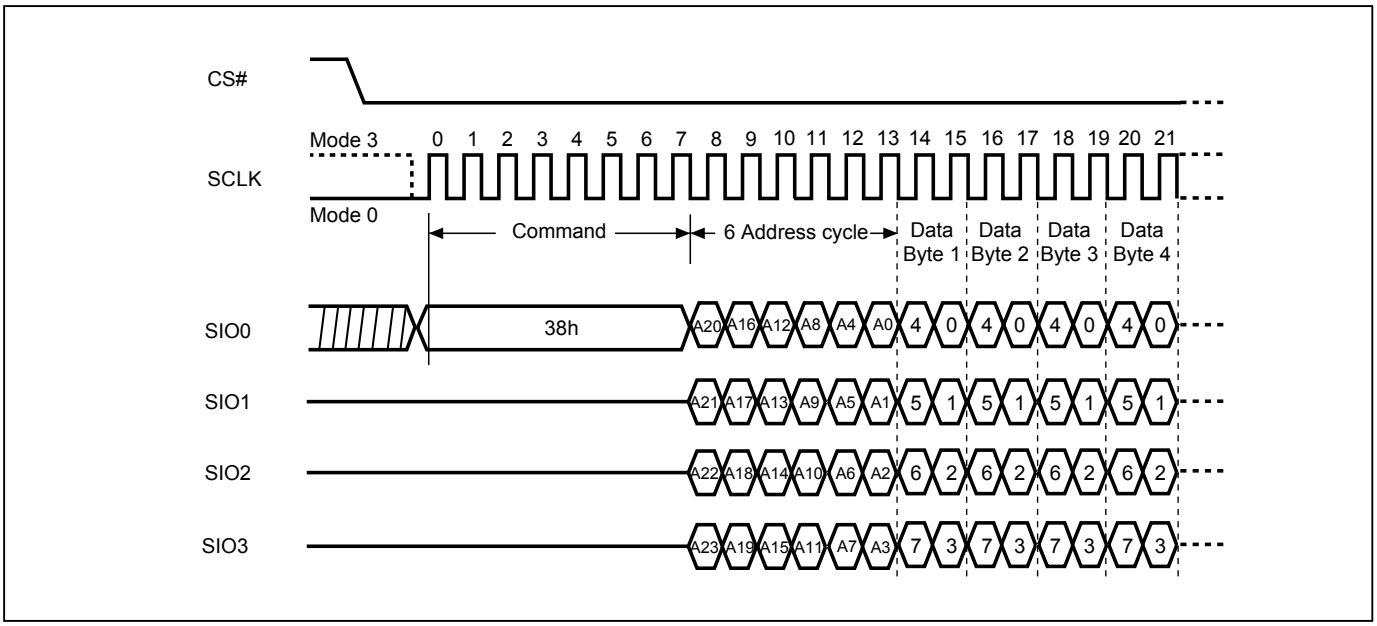
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode or to define EAR bit. To enter the 4-byte address mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte or 4-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Quad Page Program (4PP) instruction will not be executed.

Figure 81. 4 x I/O Page Program (4PP) Sequence (SPI Mode only)



Note: Please note the address cycles above are based on 3-byte address mode. For 4-byte address mode, the address cycles will be increased.

10-30. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

Figure 82. Deep Power-down (DP) Sequence (SPI Mode)

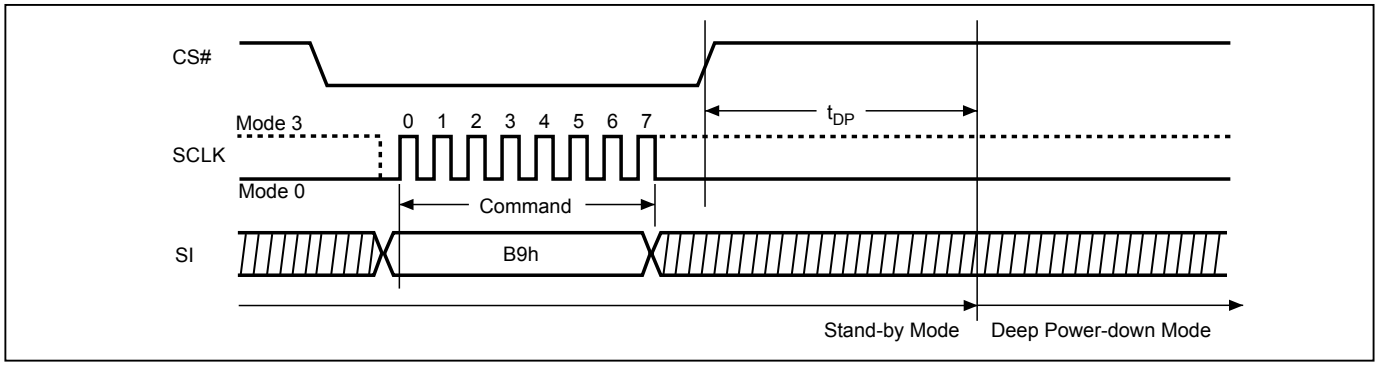
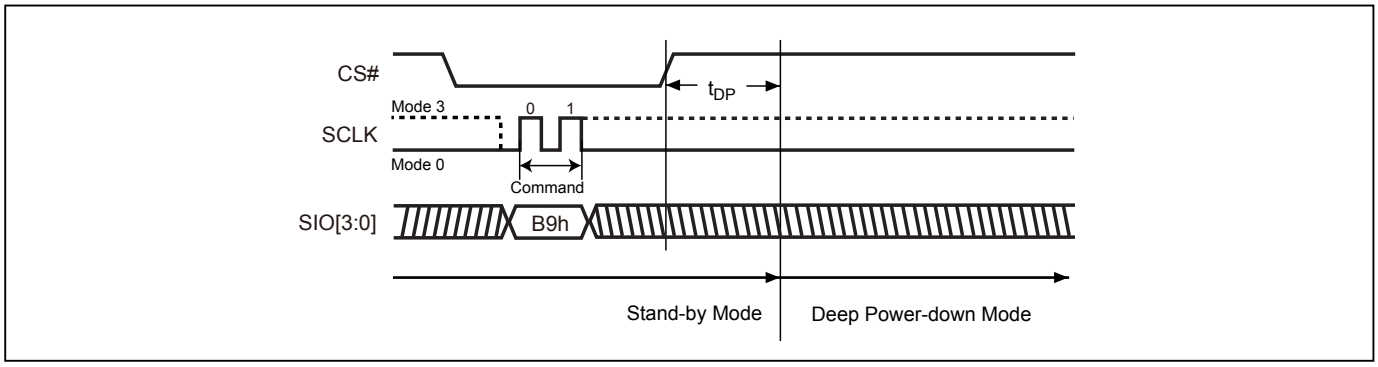


Figure 83. Deep Power-down (DP) Sequence (QPI Mode)



10-31. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 8K-bit secured OTP mode. While device is in secured OTPmode, main array access is not available. The additional 8K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

10-32. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

10-33. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

10-34. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

10-35. Write Protection Selection (WPSEL)

There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Advanced Sector Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Advanced Sector Protection mode is disabled. If WPSEL=1, Advanced Sector Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command. **Please note that the WPSEL bit is an OTP bit. Once WPSEL is set to "1", it cannot be programmed back to "0".**

When WPSEL = 0: Block Protection (BP) mode,
The memory array is write protected by the BP3~BP0 bits.

When WPSEL =1: Advanced Sector Protection mode,
Blocks are individually protected by their own SPB or DPB. On power-up, all blocks are write protected by the Dynamic Protection Bits (DPB) by default. The Advanced Sector Protection instructions WRLR, RDLR, WRPASS, RDPASS, PASSULK, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, and GBULK are activated. The BP3~BP0 bits of the Status Register are disabled and have no effect. Hardware protection is performed by driving WP#=0. Once WP#=0 all blocks and sectors are write protected regardless of the state of each SPB or DPB.

The sequence of issuing WPSEL instruction is: CS# goes low → send WPSEL instruction to enable the Advanced Sector Protect mode → CS# goes high.

Write Protection Selection

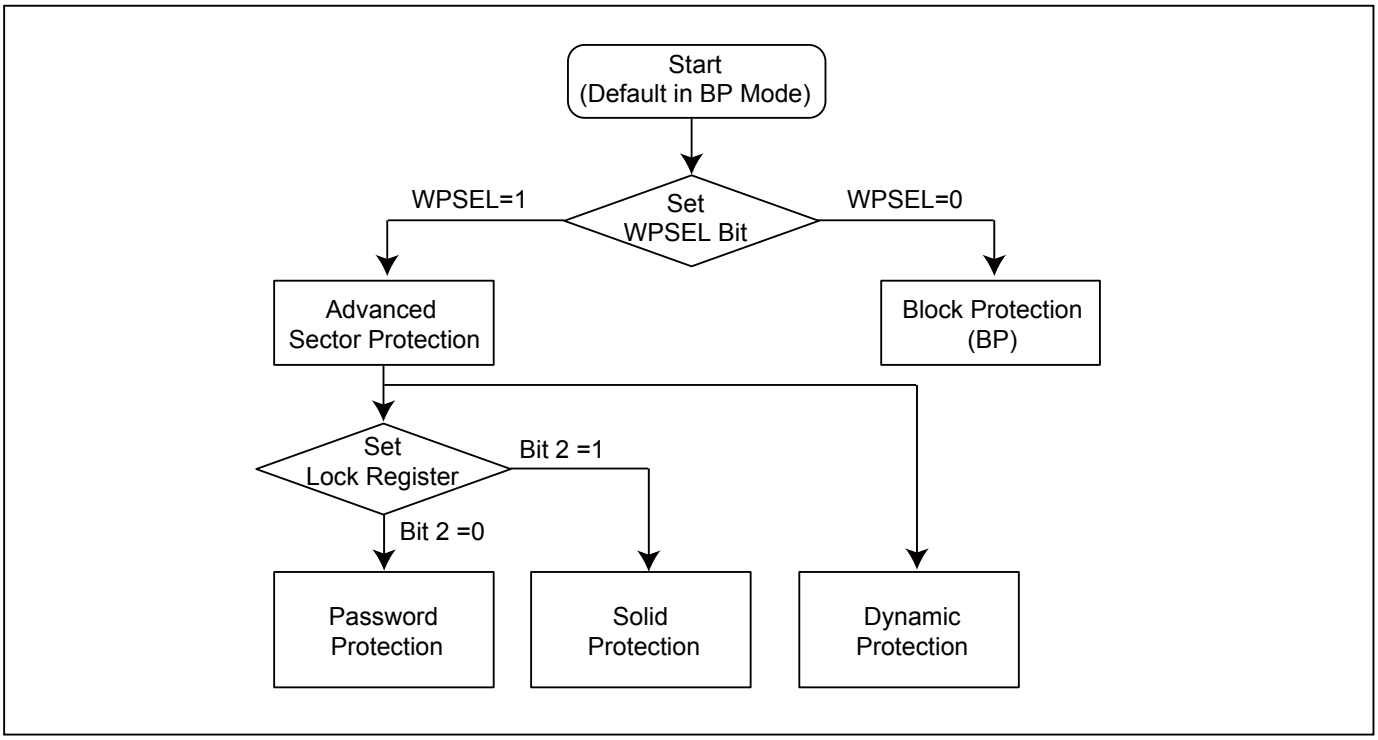
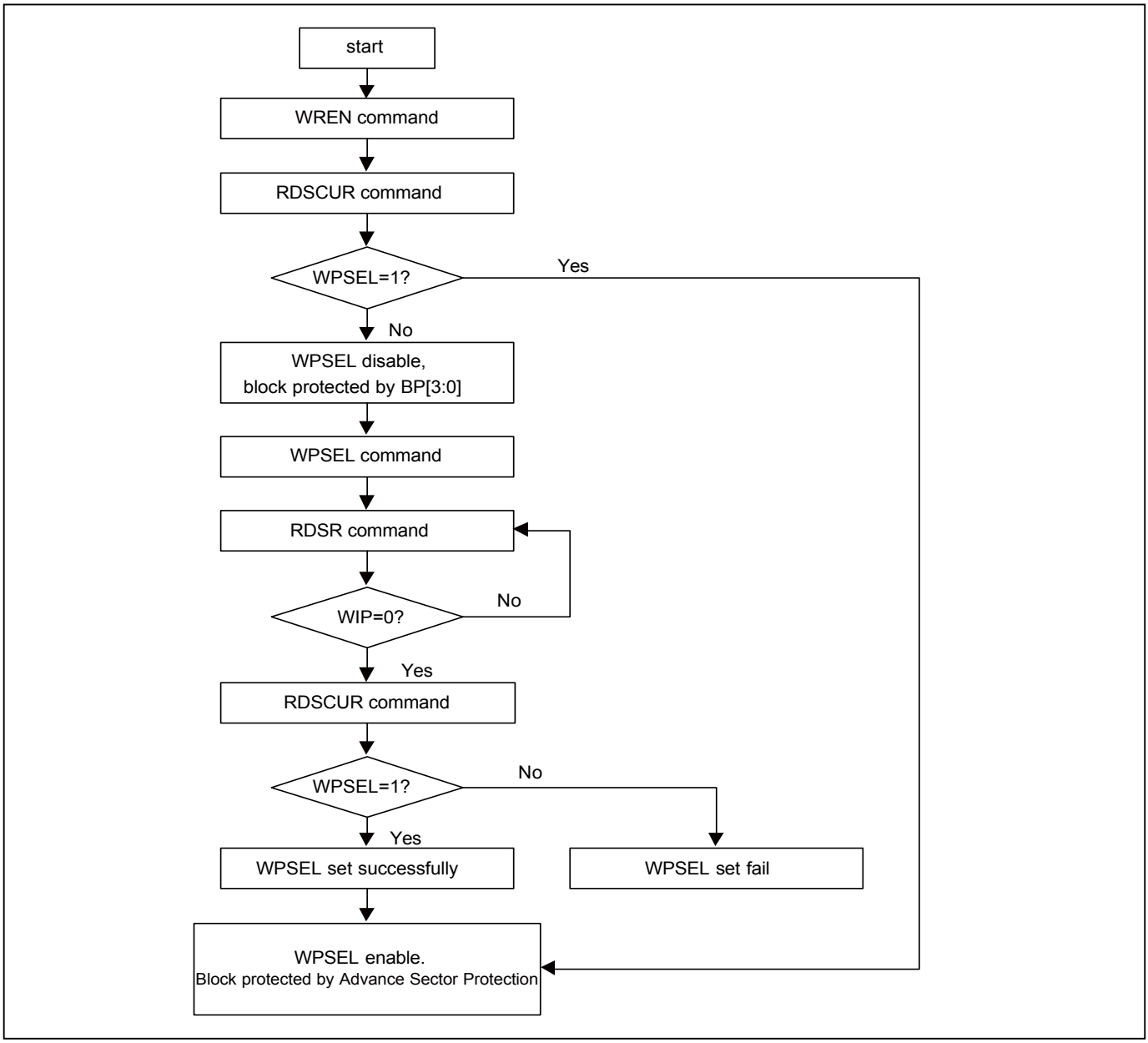


Figure 84. WPSEL Flow



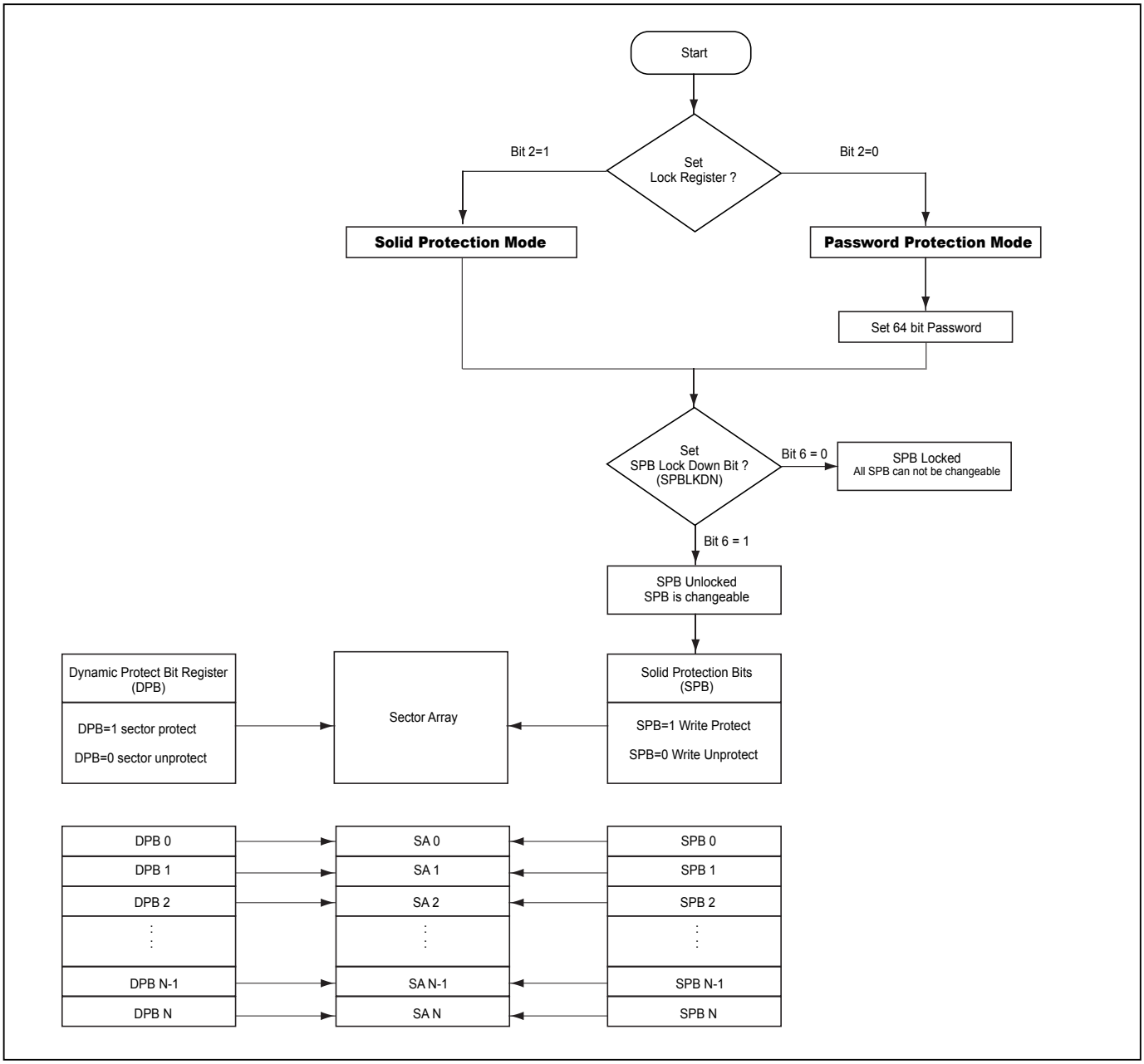
10-36. Advanced Sector Protection

There are two ways to implement software Advanced Sector Protection on this device. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or all sectors.

There is a non-volatile (SPB) and volatile (DPB) protection bit related to the single sector in main flash array. Each of the sectors is protected from programming or erasing operation when the bit is set.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory. The detail algorithm of advanced sector protection is shown as follows:

Figure 85. Advanced Sector Protection Overview



10-36-1. Lock Register

The Lock Register is a 16-bit register. Lock Register Bit[6] is SPB Lock Down Bit (SPBLKDN) which is assigned to control all SPB bit status. Lock Register Bit[2] is Password Protection Mode Lock Bit. Both bits are defaulted as 1 when shipping from factory.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed.

Users can choose their favorite sector protecting method via setting Lock Register Bit[2] using WRLR command. The device default status was in Solid Protection Mode (Bit[2]=1), Once Bit[2] has been programmed (cleared to "0"), the device will enable the Password Protection Mode and lock in that mode permanently.

In Solid Protection Mode (Bit[2]=1, factory default), the SPBLKDN can be programmed using the WRLR command and permanently lock down the SPB bits. After programming SPBLKDN to 0, all SPB can not be changed anymore, and neither Lock Register Bit[2] nor Bit[6] can be altered anymore.

In Password Protection Mode (Bit[2]=0), the SPBLKDN becomes a volatile bit with default 0 (SPB bit protected). A correct password is required with PASSULK command to set SPBLKDN to 1. To clear SPBLKDN back to 0, a Hardware/Software Reset or power-up cycle is required.

If user selects Password Protection mode, the password setting is required. User can set password by issuing WRPASS command before Lock Register Bit[2] set to 0.

Lock Register

Bits	Description	Bit Status	Default	Type
15 to 7	Reserved	Reserved		Reserved
6	SPB Lock Down bit (SPBLKDN)	0: SPB bit Protected 1: SPB bit Unprotected	Solid Protection Mode: 1 Password Protection Mode: 0	Bit 2=1: OTP Bit 2=0: Volatile
5 to 3	Reserved	Reserved		Reserved
2	Password Protection Mode Lock Bit	0=Password Protection Mode Enable 1= Solid Protection Mode	1	OTP
1 to 0	Reserved	Reserved		Reserved

Figure 86. Read Lock Register (RDLR) Sequence

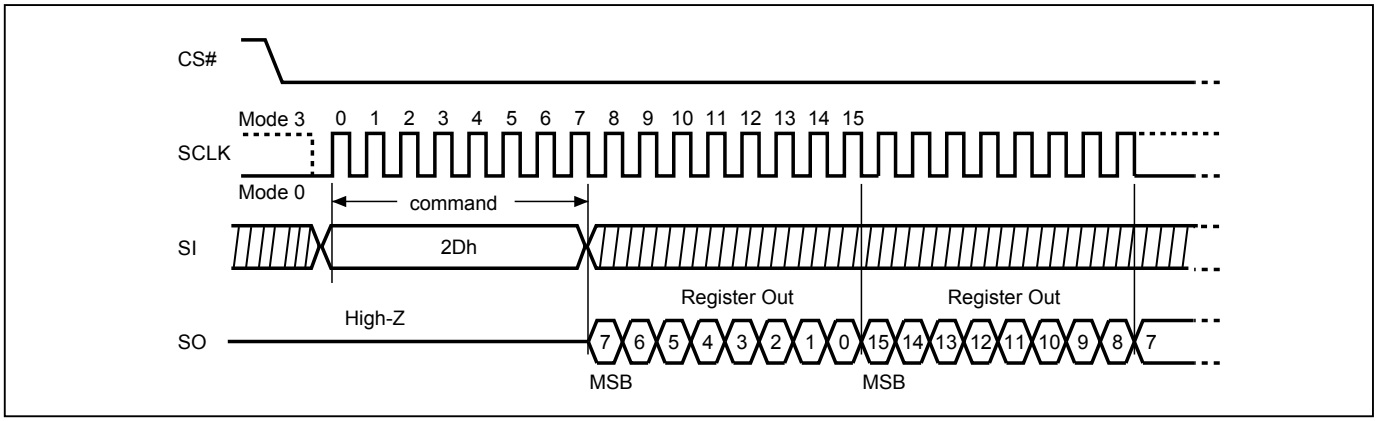
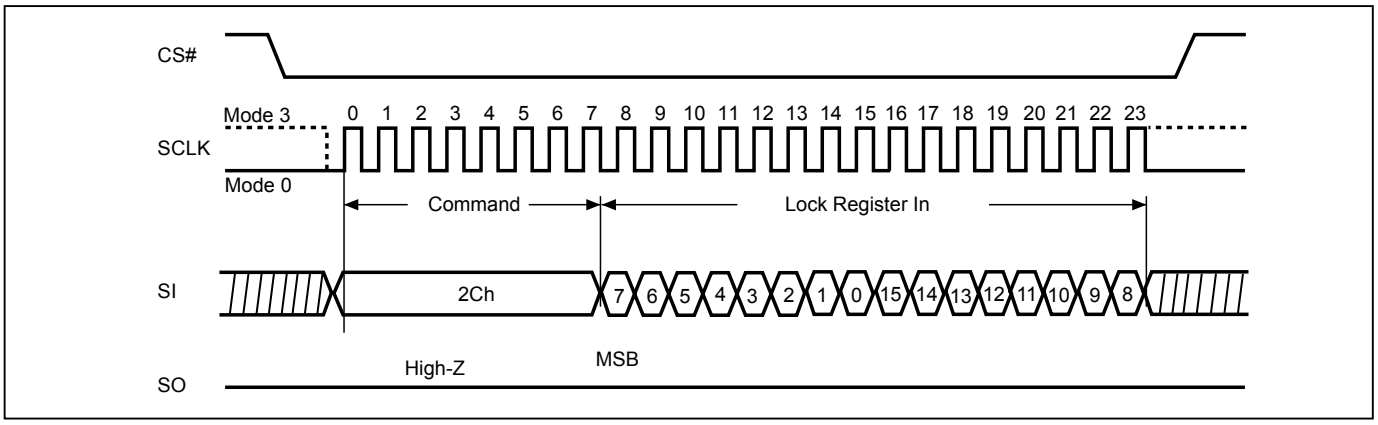


Figure 87. Write Lock Register (WRLR) Sequence (SPI Mode)



10-36-2. Solid Protection Bits

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The SPBLKDN bit must be “1” before any SPB can be modified. In Solid Protection mode the SPBLKDN bit defaults to “1” after power-on or reset. Under Password Protection mode, the SPBLKDN bit defaults to “0” after power-on or reset, and a PASSULK command with a correct password is required to set the SPBLKDN bit to “1”.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

Note: If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB (Solid protected Bit)	00h= SPB for the sector address unprotected FFh= SPB for the sector address protected	00h	Non-volatile

Figure 88. Read SPB Status (RDSPB) Sequence

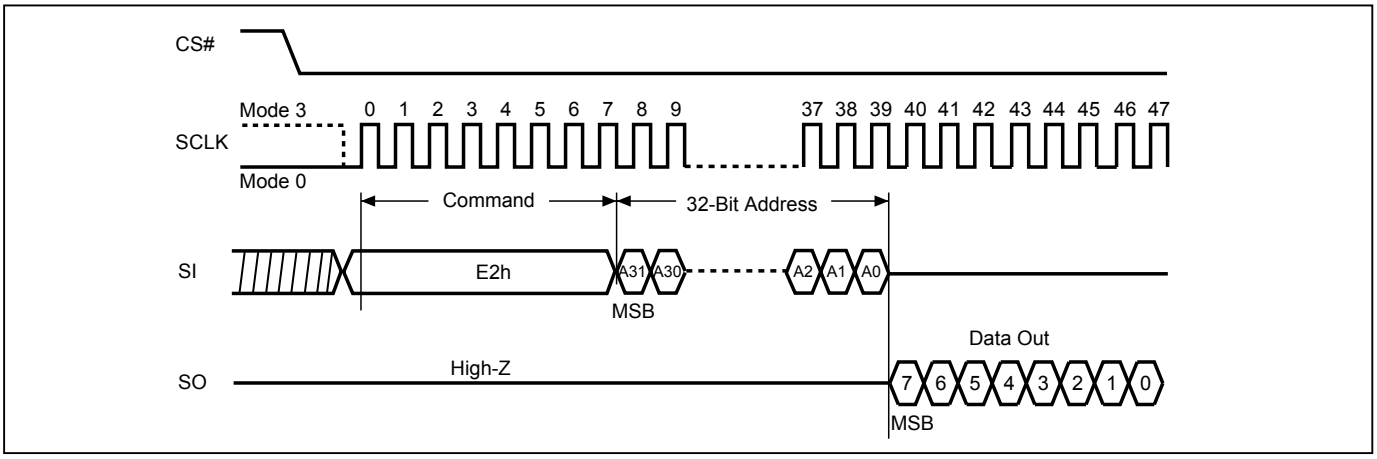


Figure 89. SPB Erase (ESSPB) Sequence

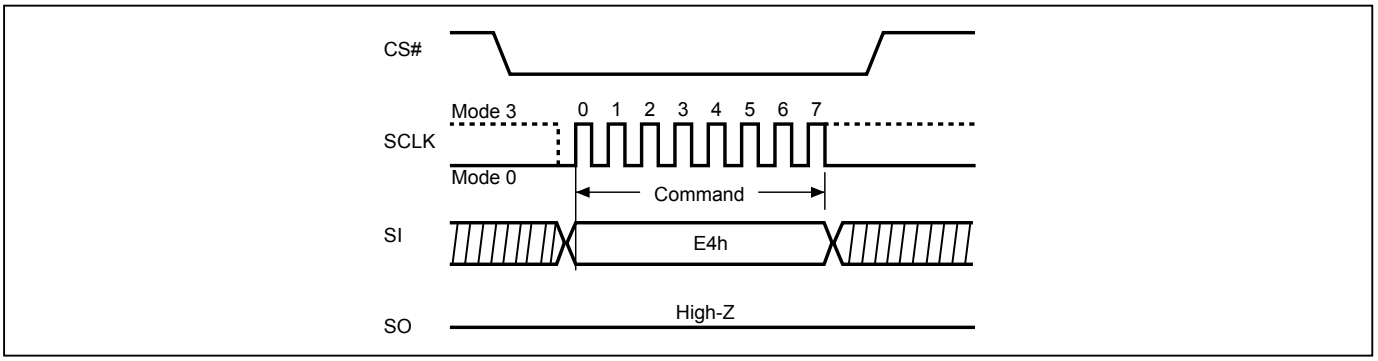
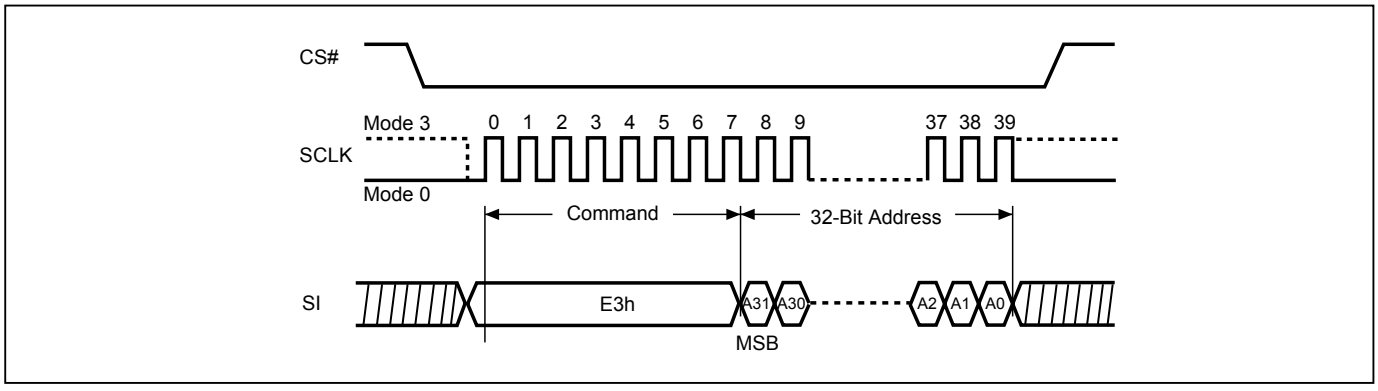


Figure 90. SPB Program (WRSPB) Sequence



10-36-3. Dynamic Write Protection Bits

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from unintentional change, and is easy to disable when there are necessary changes.

All DPBs are default as protected (FFh) after reset or upon power up cycle. Via setting up Dynamic Protection bit (DPB) by write DPB command (WRDPB), user can cancel the Dynamic Protection of associated sector.

The Dynamic Protection only works on those unprotected sectors whose SPBs are cleared. After the DPB state is cleared to “0”, the sector can be modified if the SPB state is unprotected state.

DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected FFh= DPB for the sector address protected	FFh	Volatile

Figure 91. Read DPB Register (RDDPB) Sequence

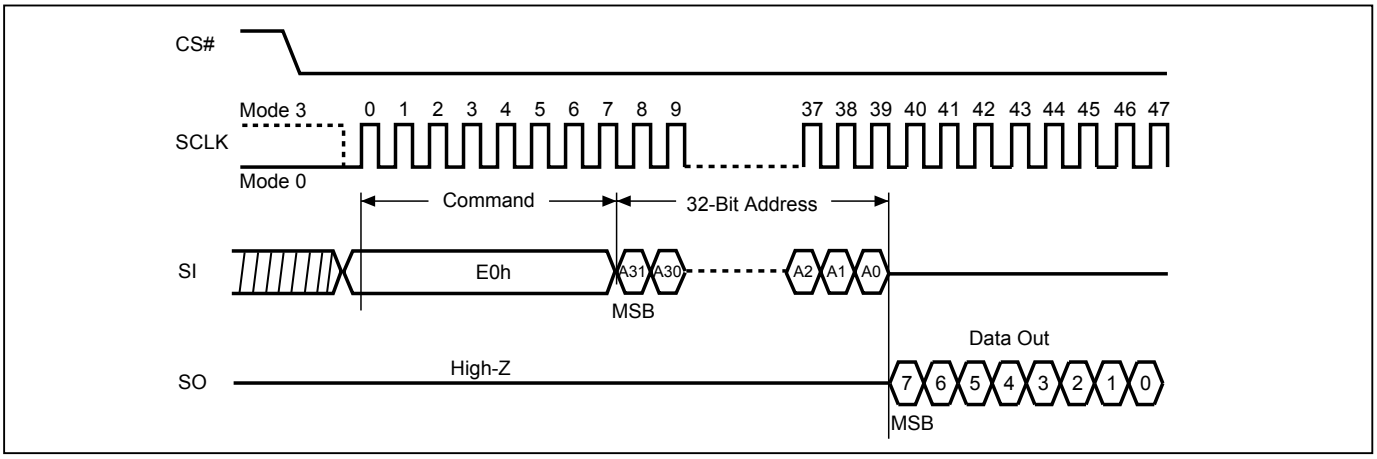
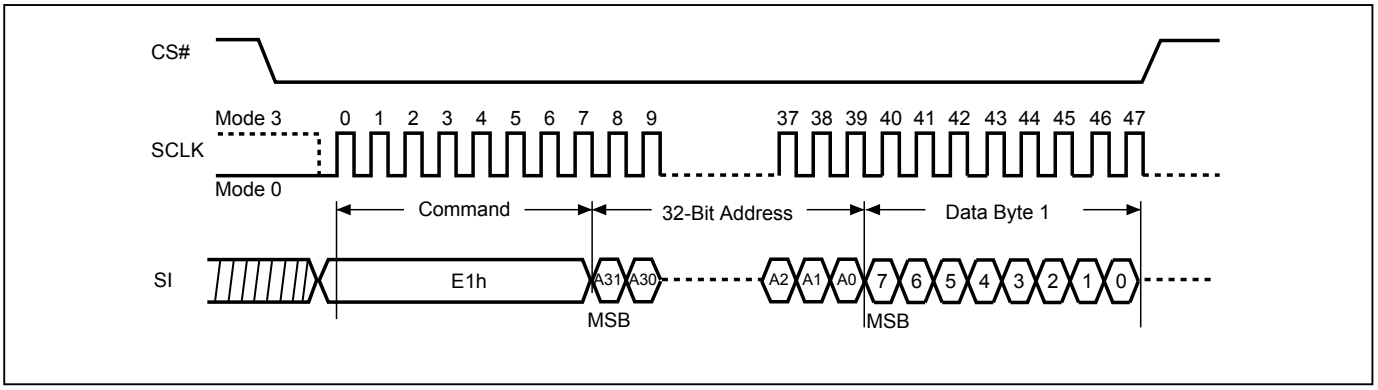


Figure 92. Write DPB Register (WRDPB) Sequence



10-36-4. Password Protection Mode

Password Protection mode potentially provides a higher level of security than Solid Protection mode. In Password Protection mode, the SPBLKDN bit defaults to “0” after a power-on cycle or reset. When SPBLKDN=0, the SPBs are locked and cannot be modified. A 64-bit password must be provided to unlock the SPBs.

The PASSULK command with the correct password will set the SPBLKDN bit to “1” and unlock the SPB bits. After the correct password is given, a wait of 2us is necessary for the SPB bits to unlock. The Status Register WIP bit will clear to “0” upon completion of the PASSULK command. Once unlocked, the SPB bits can be modified. A WREN command must be executed to set the WEL bit before sending the PASSULK command.

Several steps are required to place the device in Password Protection mode. Prior to entering the Password Protection mode, it is necessary to set the 64-bit password and verify it. The WRPASS command writes the password and the RDPASS command reads back the password. Password verification is permitted until the Password Protection Mode Lock Bit has been written to “0”. Password Protection mode is activated by programming the Password Protection Mode Lock Bit to “0”. This operation is not reversible. Once the bit is programmed, it cannot be erased. The device remains permanently in Password Protection mode and the 64-bit password can neither be retrieved nor reprogrammed.

The password is all “1’s” when shipped from the factory. The WRPASS command can only program password bits to “0”. The WRPASS command cannot program “0’s” back to “1’s”. All 64-bit password combinations are valid password options. A WREN command must be executed to set the WEL bit before sending the WRPASS command.

- The unlock operation will fail if the password provided by the PASSULK command does not match the stored password. This will set the P_FAIL bit to “1” and insert a delay before clearing the WIP bit to “0”. User has to wait 150us before issuing another PASSULK command. This restriction makes it impractical to attempt all combinations of a 64-bit password (such an effort would take millions of years). Monitor the WIP bit to determine whether the device has completed the PASSULK command.

- When a valid password is provided, the PASSULK command does not insert the delay before returning the WIP bit to zero. The SPBLKDN bit will set to “1” and the P_FAIL bit will be “0”.

- It is not possible to set the SPBLKDN bit to “1” if the password had not been set prior to the Password Protection mode being selected.

Password Register (PASS)

Bits	Field Name	Function	Type	Default State	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFFFFFFFFFFh	Non-volatile OTP storage of 64 bit password. The password is no longer readable after the Password Protection mode is selected by programming Lock Register bit 2 to zero.

Figure 93. Read Password Register (RDPASS) Sequence

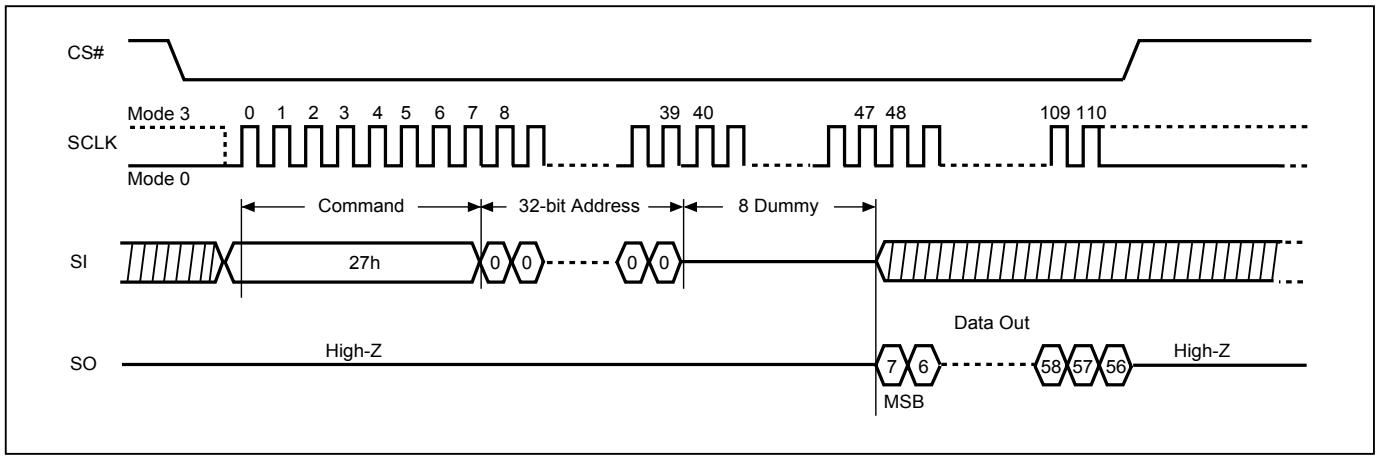


Figure 94. Write Password Register (WRPASS) Sequence

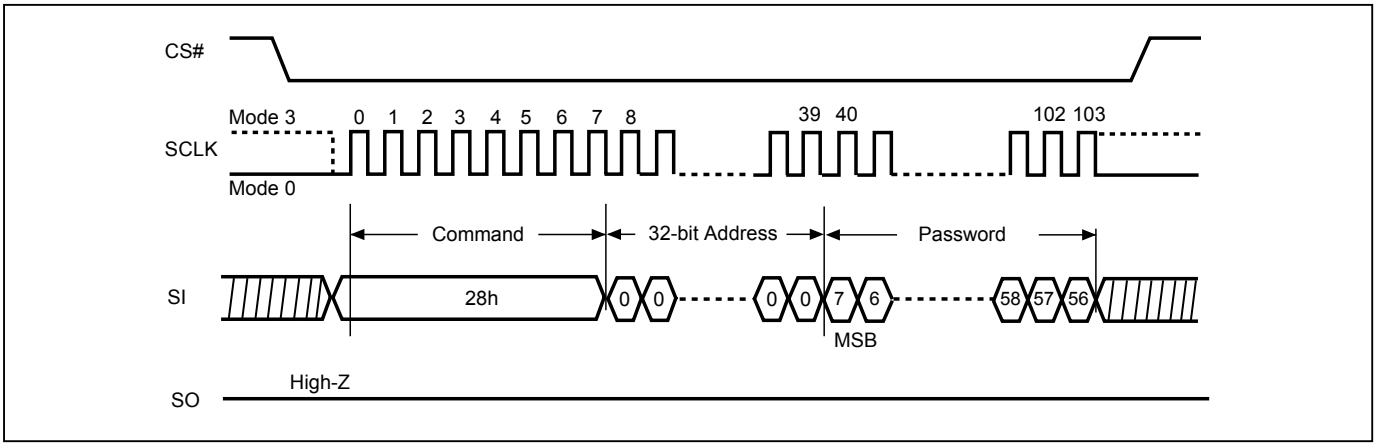
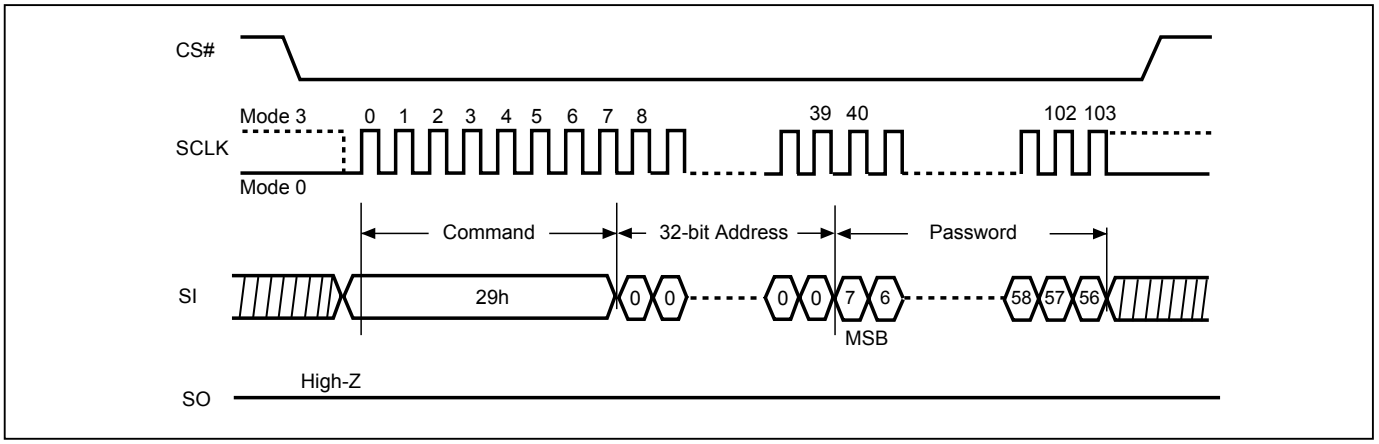


Figure 95. Password Unlock (PASSULK) Sequence



10-36-5. Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is a chip-based protected or unprotected operation. It can enable or disable all DPB.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction →CS# goes high.

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

10-36-6. Sector Protection States Summary Table

Protection Status		Sector State
DPB bit	SPB bit	
0	0	Unprotect
0	1	Protect
1	0	Protect
1	1	Protect

10-37. Program Suspend and Erase Suspend

The Suspend instruction interrupts a Program or Erase operation to allow the device conduct other operations.

After the device has entered the suspended state, the memory array can be read except for the page being programmed or the sector being erased.

Security Register bit 2 (PSB) and bit 3 (ESB) can be read to check the suspend status. The PSB (Program Suspend Bit) sets to “1” when a program operation is suspended. The ESB (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The PSB or ESB clears to “0” when the program or erase operation is resumed.

When the Serial NOR Flash receives the Suspend instruction, Program Suspend Latency(tPSL) or Erase Suspend latency(tESL) is required to complete suspend operation. (Refer to*"Table 19. AC CHARACTERISTICS"*) After the device has entered the suspended state, the WEL bit is clears to “0” and the PSB or ESB in security register is set to “1”, then the device is ready to acceptanother command.

However, some commands can be executed without tPSL or tESL latency during the program/erase suspend, and can be issued at any time during the Suspend.

Please refer to *"Table 13. Acceptable Commands During Suspend".*

Figure 96. Suspend to Read Latency

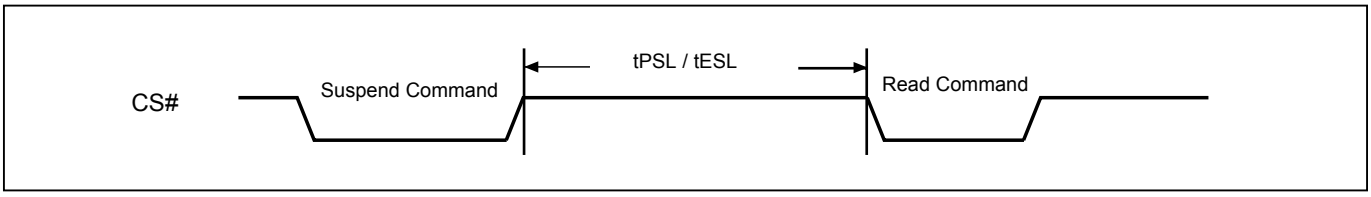


Table 13. Acceptable Commands During Suspend

Command Name	Command Code	Suspend Type	
		Program Suspend	Erase Suspend
Commands which require tPSL/tESL delay			
READ	03h	•	•
FAST READ	0Bh	•	•
2READ	BBh	•	•
DREAD	3Bh	•	•
4READ	EBh	•	•
QREAD	6Bh	•	•
4READ4B	ECh	•	•
4DTRD	EDh	•	•
4DTRD4B	EEh	•	•
FASTREAD4B	0Ch	•	•
2READ4B	BCh	•	•
DREAD4B	3Ch	•	•
RDSFDP	5Ah	•	•
RDID	9Fh	•	•
QPIID	AFh	•	•
SBL	C0h	•	•
ENSO	B1h	•	•
EXSO	C1h	•	•
WREN	06h	•	•
RESUME	30h	•	•
RDLR	2Dh	•	•
RDSPB	E2h	•	•
RDFBR	16h	•	•
RDDPB	E0h	•	•
EQIO	35h	•	•
RSTQIO	F5h	•	•
REMS	90h	•	•
Commands not required tPSL/tESL delay			
WRDI	04h	•	•
RDSR	05h	•	•
RDCR	15h	•	•
RDSCUR	2Bh	•	•
RES	ABh	•	•
RSTEN	66h	•	•
RST	99h	•	•
NOP	00h	•	•

10-38. Program Resume and Erase Resume

The Resume instruction resumes a suspended Program or Erase operation. After the device receives the Resume instruction, the WEL and WIP bits are set to “1” and the PSB or ESB is cleared to “0”.The program or erase operation will continue until it is completed or until another Suspend instruction is received.

To issue another Suspend instruction, the minimum resume-to-suspend latency (tPRS or tERS) is required. However, in order to finish the program or erase progress, a period equal to or longer than the typical timing is required.

To issue other command except suspend instruction, a latency of the self-timed Page Program Cycle time (tPP) or Sector Erase (tSE) is required. The WEL and WIP bits are cleared to “0” after the Program or Erase operation is completed.

Note:
The Resume instruction will be ignored during Performance Enhance Mode. Make sure the Serial NOR Flash has exited the Performance Enhance Mode before issuing the Resume instruction.

Figure 97. Resume to Read Latency

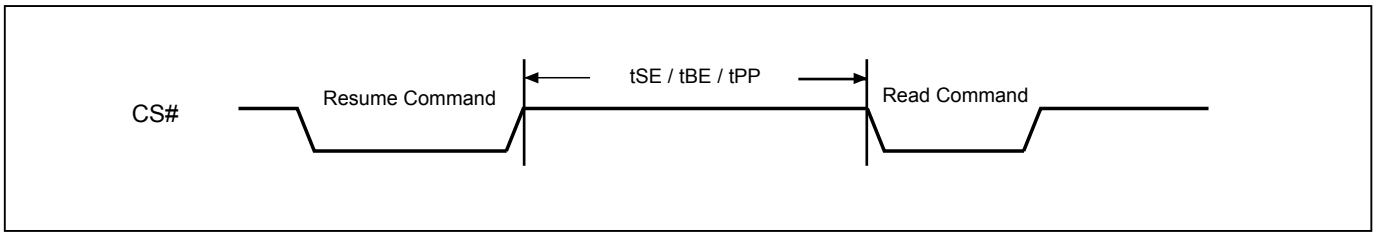
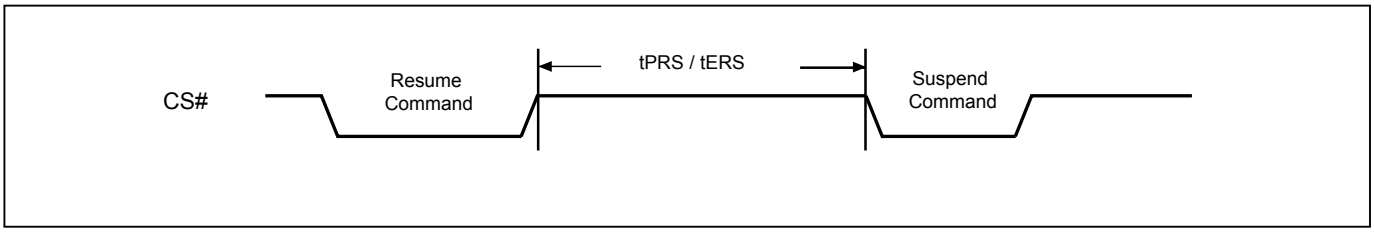


Figure 98. Resume to Suspend Latency



10-39. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care during SPI mode.

10-40. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command and Reset (RST) command. It returns the device to standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

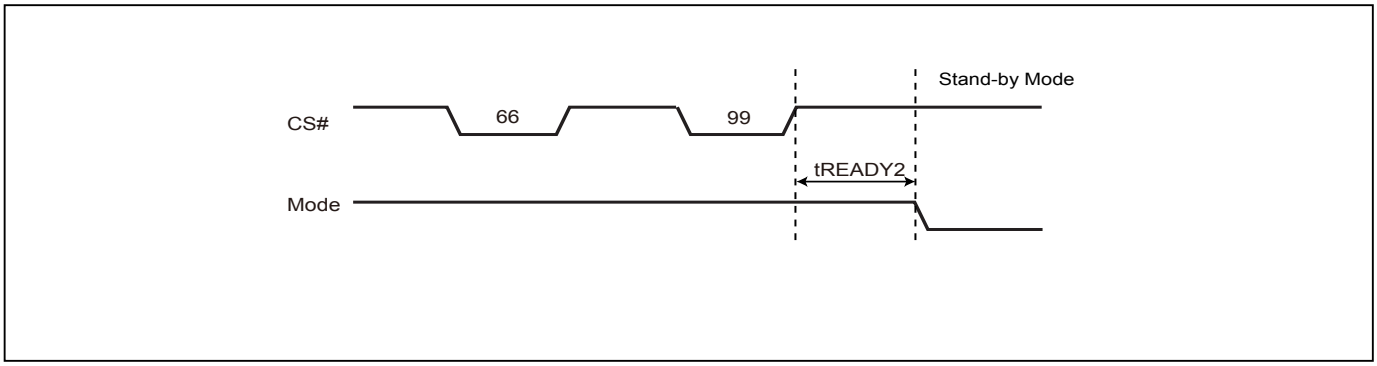
To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

Both SPI (8 clocks) and QPI (2 clocks) command cycle can accept by this instruction. The SIO[3:1] are don't care when during SPI mode.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 15. Reset Timing-(Other Operation)"* for tREADY2.

Figure 99. Software Reset Recovery



Note: Refer to *"Table 15. Reset Timing-(Other Operation)"* for tREADY2.

Figure 100. Reset Sequence (SPI mode)

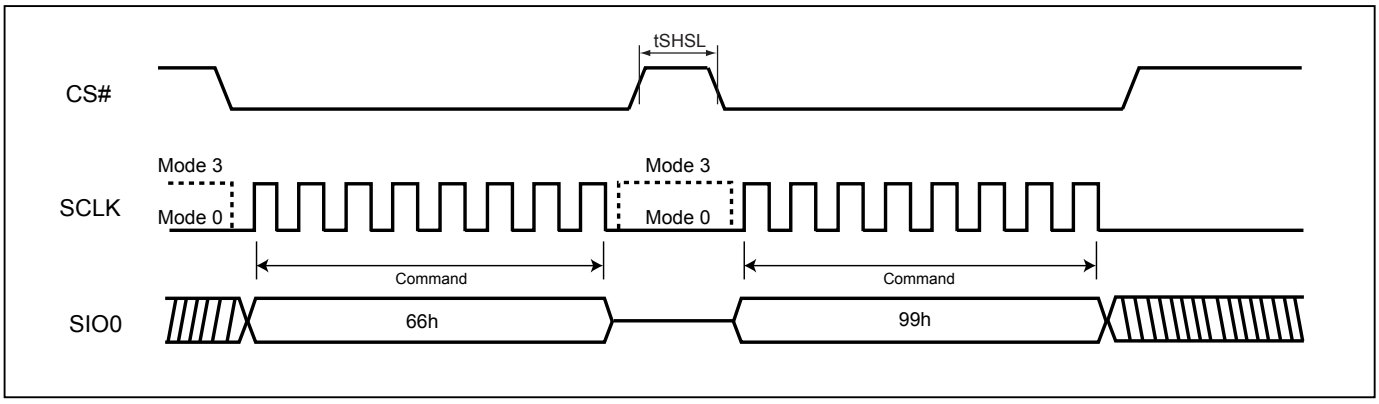
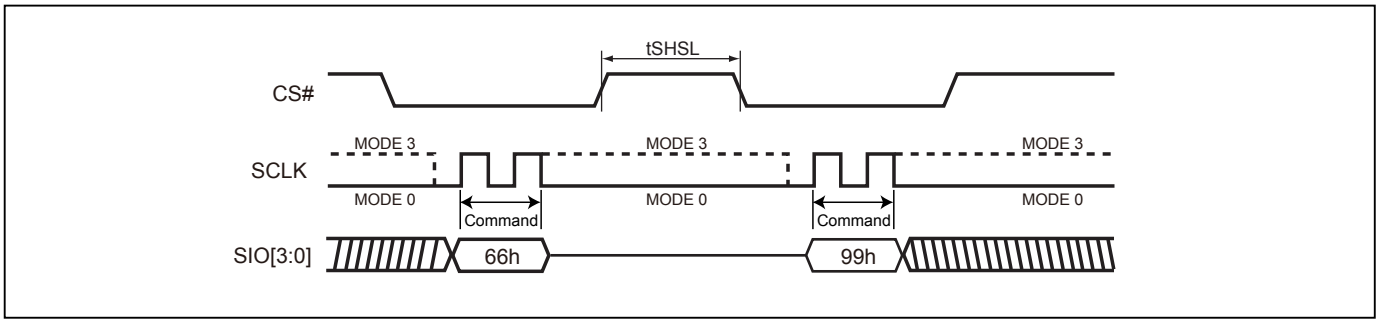


Figure 101. Reset Sequence (QPI mode)



11. Serial Flash Discoverable Parameter (SFDP)

11-1. Read SFDP Mode (RDSFDP)

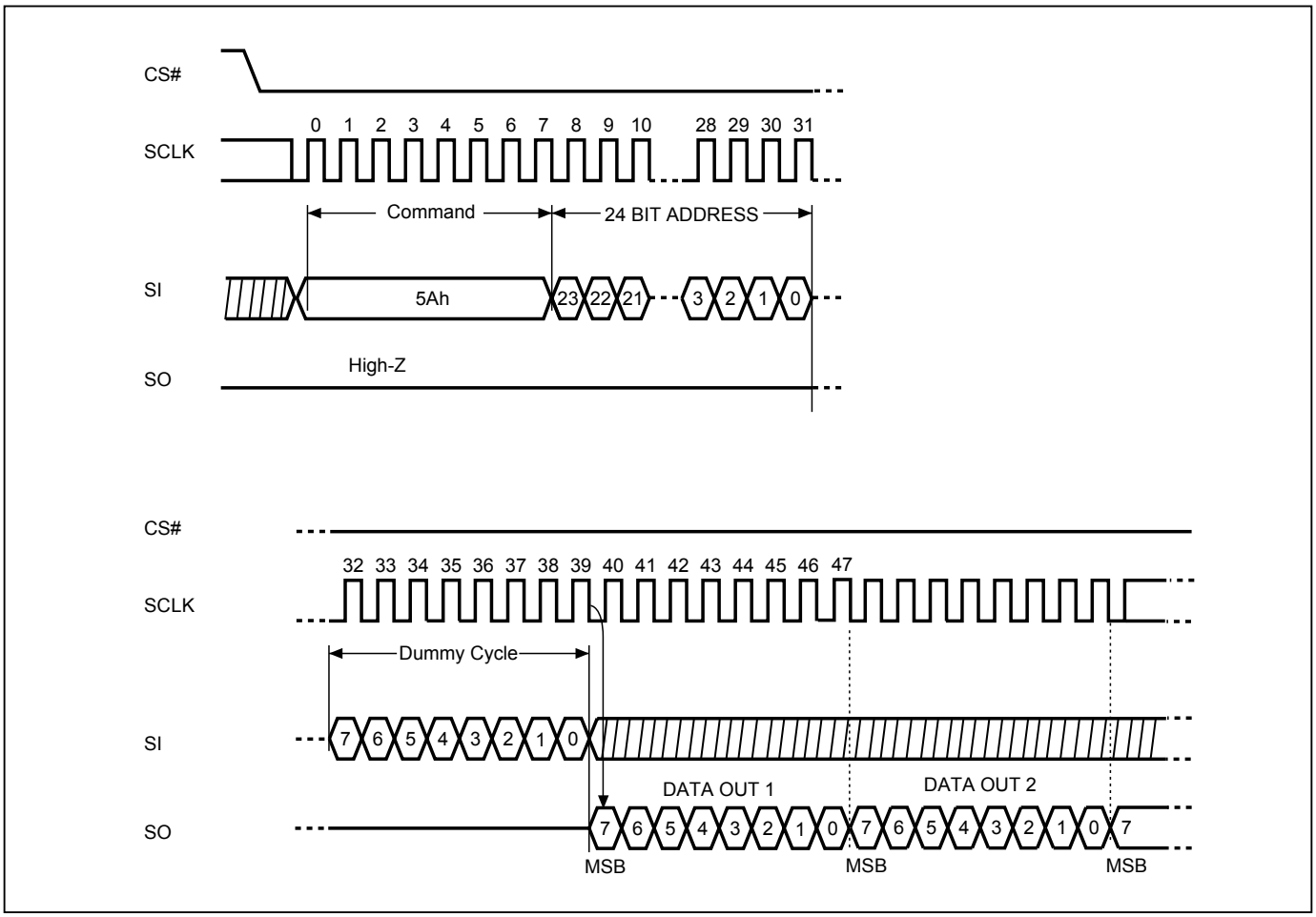
The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216B.

For SFDP register values detail, please contact local Macronix sales channel for Application Note.

Figure 102. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence



12. RESET

Driving the RESET# pin low for a period of tRLRH or longer will reset the device. After reset cycle, the device is at the following states:
- Standby mode
- All the volatile bits such as WEL/WIP/SRAM lock bit will return to the default status as power on.
- 3-byte address mode

If the device is under programming or erasing, driving the RESET# pin low will also terminate the operation and data could be lost. During the resetting cycle, the SO data becomes high impedance and the current will be reduced to minimum.

Figure 103. RESET Timing

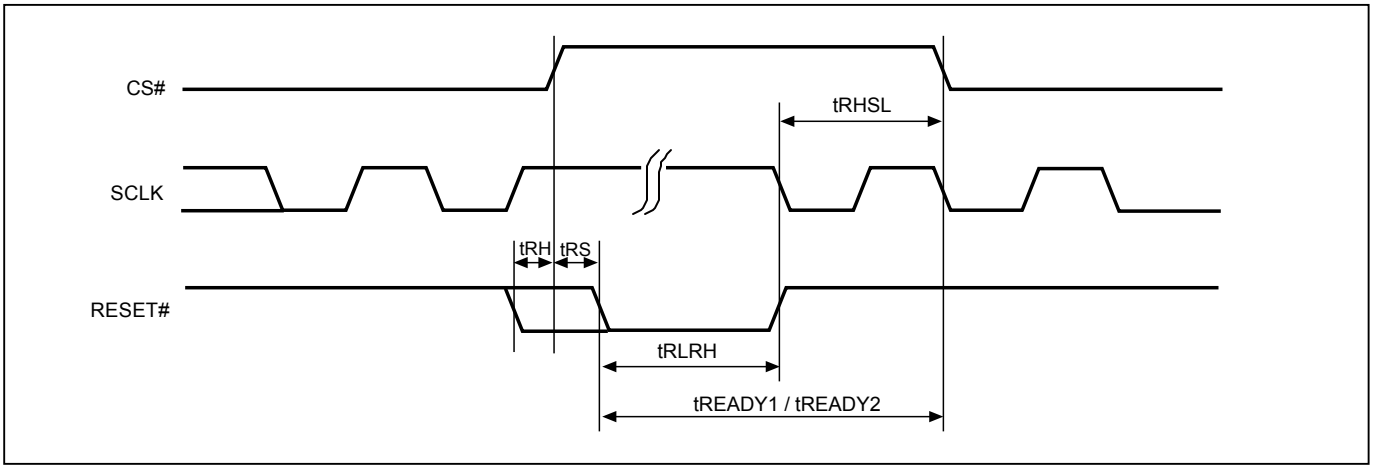


Table 14. Reset Timing-(Power On)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY1	Reset Recovery time	35			us

Table 15. Reset Timing-(Other Operation)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tRHSL	Reset# high before CS# low	10			us
tRS	Reset# setup time	15			ns
tRH	Reset# hold time	15			ns
tRLRH	Reset# low pulse width	10			us
tREADY2	Reset Recovery time (During instruction decoding)	40			us
	Reset Recovery time (for read operation)	40			us
	Reset Recovery time (for program operation)	310			us
	Reset Recovery time(for SE4KB operation)	12			ms
	Reset Recovery time (for BE64K/BE32KB operation)	25			ms
	Reset Recovery time (for Chip Erase operation)	1000			ms
	Reset Recovery time (for WRSR operation)	40			ms

13. POWER-ON STATE

The device is at below states when power-up:
- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:
- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The write, erase, and program command should be sent after the below time delay:
- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.
Please refer to the "*power-up timing*".

Note:
- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

14. ELECTRICAL SPECIFICATIONS

Table 16. ABSOLUTE MAXIMUM RATINGS

Rating		Value
Ambient Operating Temperature	Industrial (J) grade	-40°C to 105°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 2.5V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot to VCC+1.0V or -1.0V for period up to 20ns.

Figure 104. Maximum Negative Overshoot Waveform

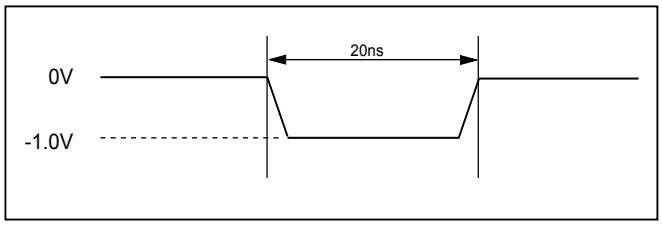


Figure 105. Maximum Positive Overshoot Waveform

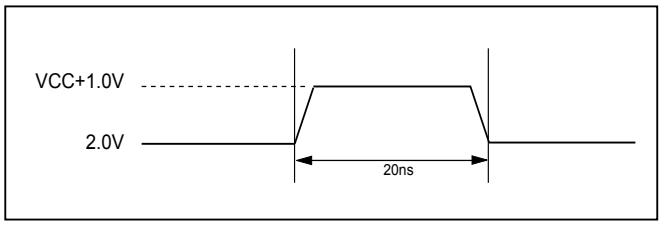
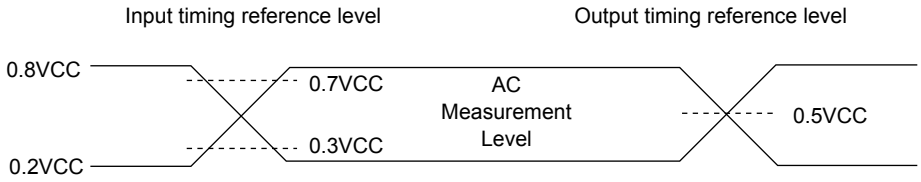


Table 17. CAPACITANCE TA = 25°C, f = 1.0 MHz

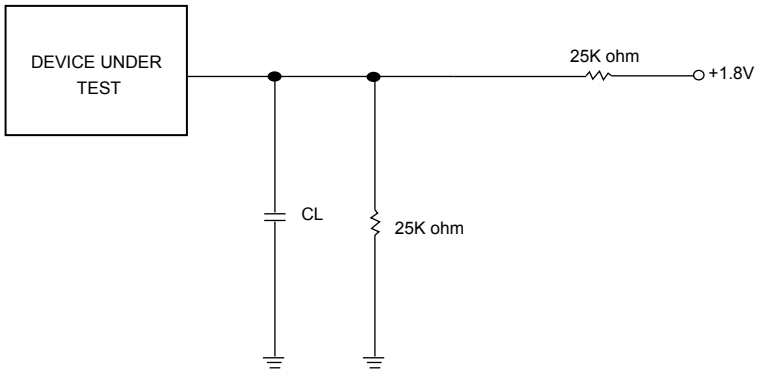
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			32	pF	VIN = 0V
COUT	Output Capacitance			32	pF	VOUT = 0V

Figure 106. DATA INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <1ns

Figure 107. OUTPUT LOADING



CL=30pF Including jig capacitance

Figure 108. SCLK TIMING DEFINITION

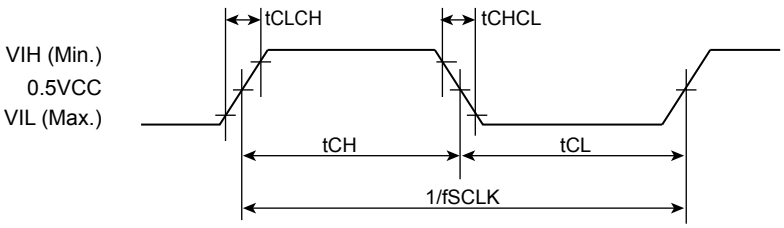


Table 18. DC CHARACTERISTICS

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±4	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±4	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		80	1000	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			12	360	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read (Note 3)	1		90	150	mA	f=83MHz, (DTR 4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				88	140	mA	f=133MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				72	120	mA	f=104MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				52	80	mA	f=84MHz, (1x I/O & 2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		30	40	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			60	160	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		20	40	mA	Erase in Progress, CS#=VCC
ICC4	VCC Block (32K, 64K) Erase Current (BE32K/BE)	1		30	40	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		80	160	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.4		0.3VCC	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 1.8V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. Pattern = Blank

Table 19. AC CHARACTERISTICS

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for all commands(except Read Operation)			D.C.		133	MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
fTSCLK		Clock Frequency for FAST READ, DREAD, 2READ, QREAD, 4READ, 4DTRD			see *"Dummy Cycle and Frequency Table (MHz)"*			MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK)		45% x (1/fSCLK)			ns
			Normal Read (fRSCLK)		7			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK)		45% x (1/fSCLK)			ns
			Normal Read (fRSCLK)		7			ns
tCLCH		Clock Rise Time (peak to peak)			0.1			V/ns
tCHCL		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			4.5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			4			ns
tDVCH/ tDVCL	tDSU	Data In Setup Time		STR	1.5			ns
				DTR	1.5			ns
tCHDX/ tCLDX	tDH	Data In Hold Time		STR	1.5			ns
				DTR	1.5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			3			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			3			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read		7			ns
			From Write/Erase/Program to Read Status Register		30			ns
tSHQZ	tDIS	Output Disable Time					8	ns
tCLQV	tV	Clock Low to Output Valid	24 BGA	Loading: 30pF			6.5	ns
				Loading: 15pF			6.5	ns
				Loading: 10pF			6.5	ns
tCLQX	tHO	Output Hold Time			1		3	ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tDP		CS# High to Deep Power-down Mode					10	us
tRES1		CS# High to Standby Mode without Electronic Signature Read					30	us
tRES2		CS# High to Standby Mode with Electronic Signature Read					30	us
tW		Write Status/Configuration Register Cycle Time					40	ms
tWREAW		Write Extended Address Register and configuration register2 volatile bit				40		ns
tPP		Page Program Cycle Time				0.15	4	ms
tSE		Sector Erase Cycle Time				25	480	ms
tBE32		Block Erase (32KB) Cycle Time				150	1100	ms
tBE		Block Erase (64KB) Cycle Time				250	2200	ms
tCE		Chip Erase Cycle Time				150	400	s
tESL(6)		Erase Suspend Latency					35	us
tPSL(6)		Program Suspend Latency					25	us
tPRS(7)		Latency between Program Resume and next Suspend			0.3	125		us
tERS(8)		Latency between Erase Resume and next Suspend			0.3	400		us

Notes:

1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Test condition is shown as *Figure 106* and *Figure 107*.
5. While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes.
6. By default dummy cycle value. Please refer to the *"Table 1. Read performance Comparison"*.
7. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
8. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
9. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.

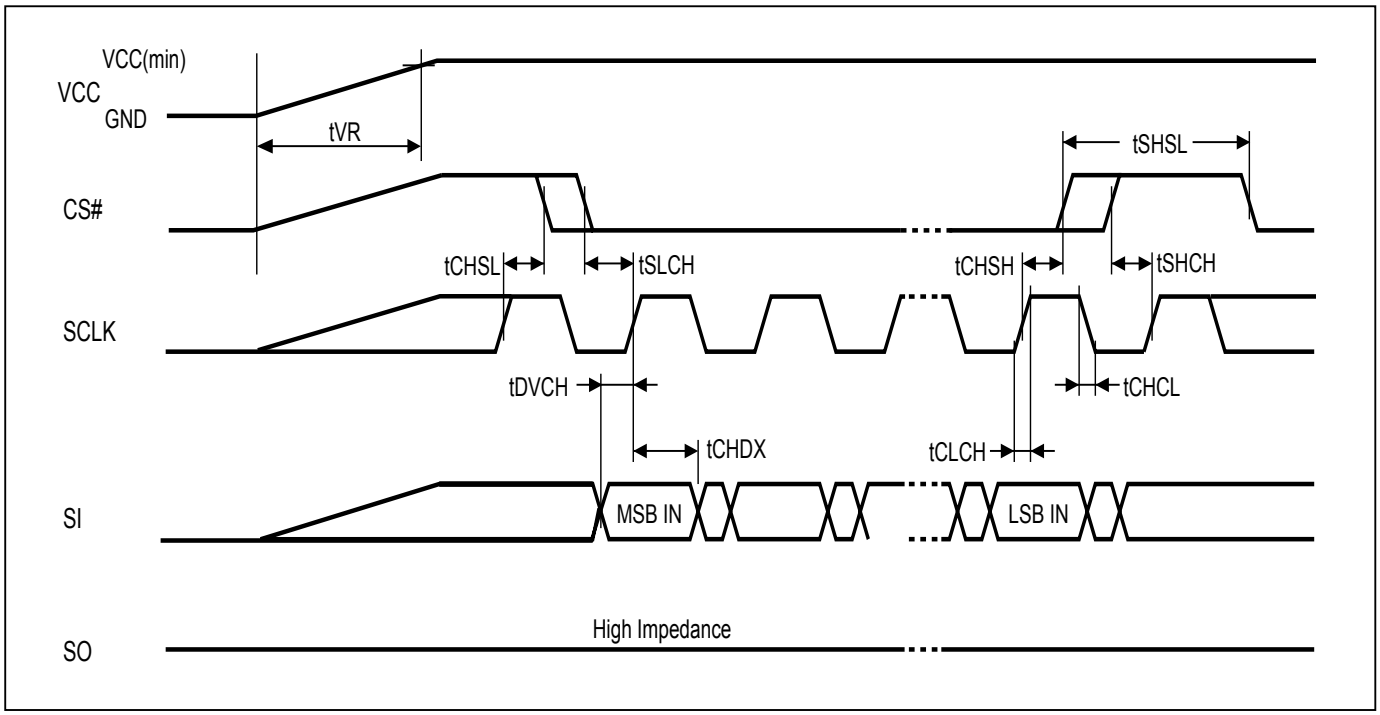
15. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *Figure 109* and *Figure 110* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 109. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1		500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *Table 19.* AC CHARACTERISTICS.

Figure 110. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

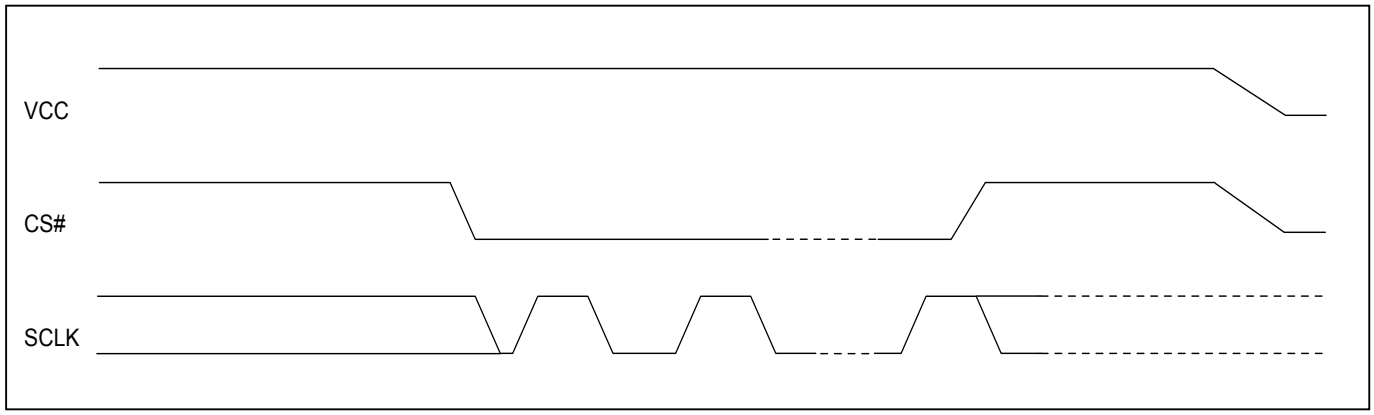


Figure 111. Power-up Timing

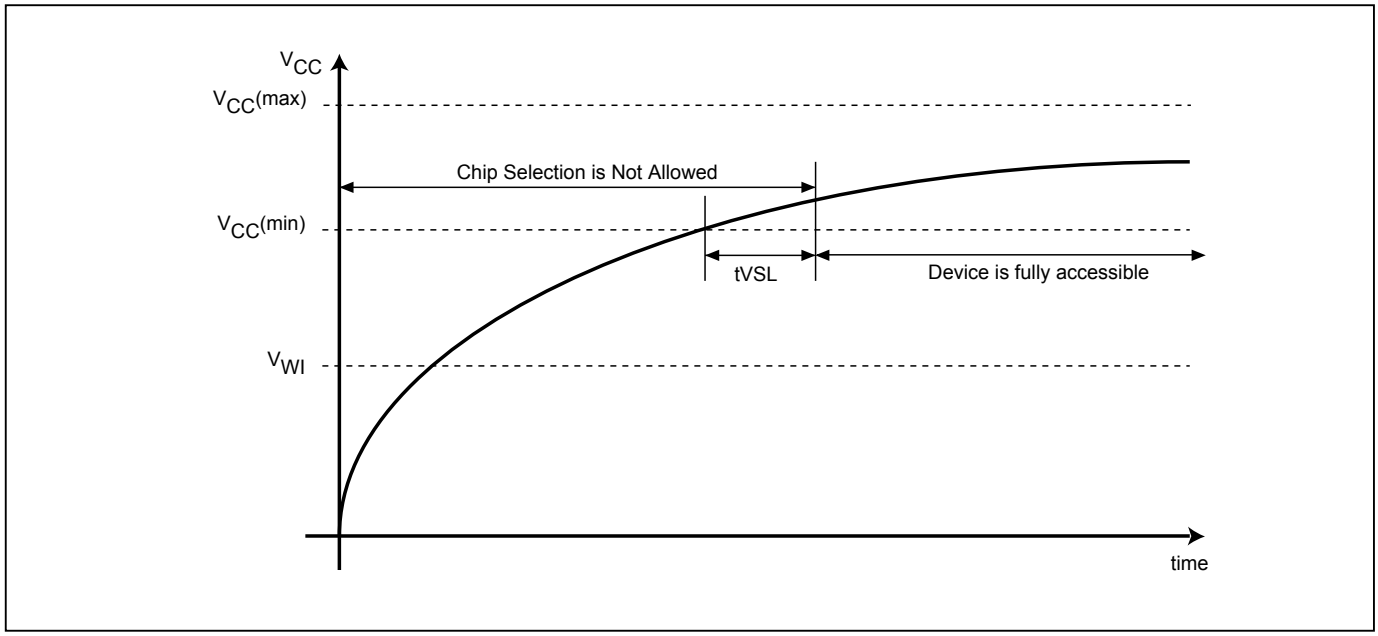


Figure 112. Power Up/Down and Voltage Drop

When powering down the device, VCC must drop below V_{PWD} for at least tPWD to ensure the device will initialize correctly during power up. Please refer to *"Figure 112. Power Up/Down and Voltage Drop"* and *"Table 20. Power-Up/Down Voltage and Timing"* below for more details.

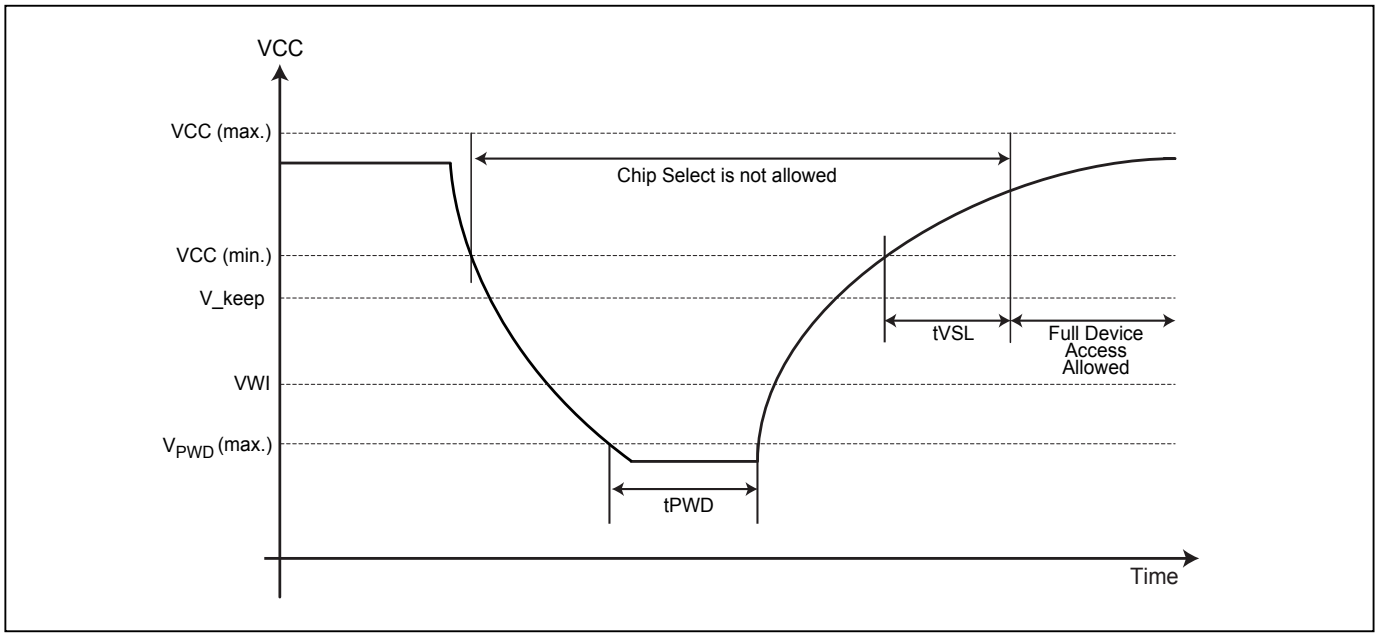


Table 20. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.8	V
V_keep	Voltage that a re-initialization is necessary if VDD drop below to VKEEP	1.5		V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVSL	VCC(min.) to device operation	3000		us
VCC	VCC Power Supply	1.7	2.0	V
VWI	Write Inhibit Voltage	1.0	1.5	V

Note: These parameters are characterized only.

15-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

16. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		25	480	ms
Block Erase Cycle Time (32KB)		150	1100	ms
Block Erase Cycle Time (64KB)		250	2200	ms
Chip Erase Cycle Time		150	400	s
Page Program Time		0.15	4	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 1.8V, and checkerboard pattern.
2. Under worst conditions of minimum operation voltage and the temperature of the worst case.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

17. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

18. LATCH-UP CHARACTERISTICS

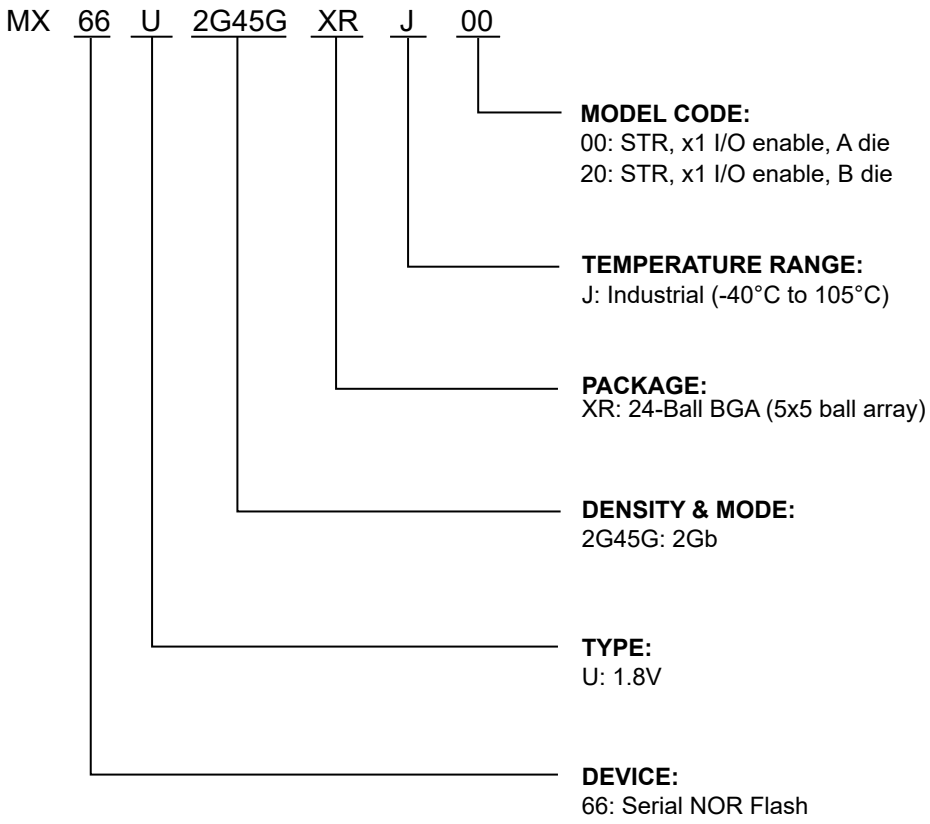
	Min.	Max.
Input Voltage with respect to GND on all power pins		1.5 VCCmax
Input Current on all non-power pins	-100mA	+100mA
Test conditions: VCC = VCCmax, one pin at a time (compliant to JEDEC JESD78 standard).		

19. ORDERING INFORMATION

Please refer to the individual product pages of Macronix Website or contact Macronix regional Sales for the latest Full Part Numbers and available form factor selection.

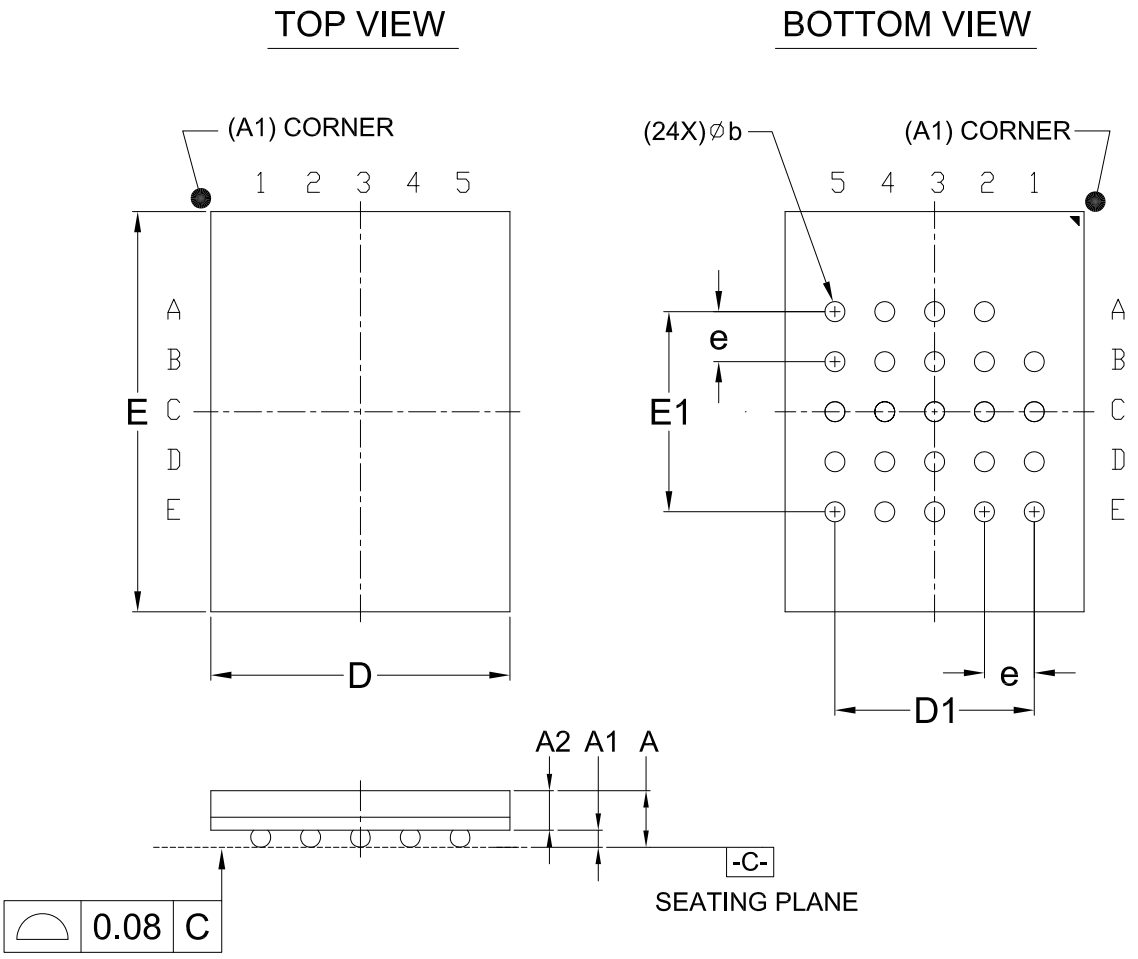
PART NO.	TEMPERATURE	PACKAGE	Remark
MX66U2G45GXRJ00	-40°C to 105°C	24-Ball BGA (5x5 ball array)	A die
MX66U2G45GXRJ20	-40°C to 105°C	24-Ball BGA (5x5 ball array)	B die

20. PART NAME DESCRIPTION



21. PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 24BALL (6x8x1.3MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.75	0.35	5.90	--	7.90	---	---
	Nom.	---	0.30	--	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.30	0.35	--	0.45	6.10	--	8.10	---	---
Inch	Min.	--	0.010	0.030	0.014	0.232	--	0.311	---	---
	Nom.	--	0.012	--	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.051	0.014	--	0.018	0.240	--	0.319	---	---

22. REVISION HISTORY

Revision	Descriptions	Page
May 07, 2018		
0.00	1. Initial Release.	All
September 03, 2018		
1.0	1. Removed "Advanced Information" to align with the product status	ALL
	2. Modified Note 2 of Erase and Programming Performance Table.	P107
August 14, 2020		
1.1	1. Modified LATCH-UP testing descriptions.	P108
	2. Modified Serial Input Timing (STR mode/DTR mode)	P14
	3. Added tDVCL and tCLDX values	P103
	4. Added "Support Performance Enhance Mode - XIP (execute-in-place)"	P5,64
	5. Corrected "Read Electronic Signature (RES) Sequence"	P33,34
	6. Added 75h and 7Ah for PGM/ERS Suspend and PGM/ERS Resume	P23
	7. Modified "Program Suspend and Erase Suspend" description	P92
	8. Modified ICC3 (Typ.) values.	P102
July 06, 2026		
1.2	1. Added Part No. : MX66U2G45GXRJ20 and Ordering descriptions modification.	P109, 110

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