



MACRONIX
INTERNATIONAL Co., LTD.

MX69GL126F

Industrial Temperature, 3 Volt, MCP Products - Parallel NOR Flash + Pseudo Static RAM (pSRAM)

**128Mb Page Mode Flash Memory (8M x 16Bit) and
32Mb pSRAM (2M x 16Bit)**

MX69GL126F (Uniform Sector)

MCP FEATURES

- **Supply Voltage of 2.7 to 3.6 Voltage**
- **Speed**
 - Flash:
 - 128Mb: 90ns
 - pSRAM: 70ns
- **Package**
 - 7x9x1.2mm 56 Ball FBGA
- **Operating Temperature Range**
 - Industrial, -40°C to +85°C

Flash Memory General Features

- Sector architecture
 - MX69GL126F uniform sector, Lowest Address Sector Protected (Protection when WP#=VIL): 128 x 64Kword(128KB)
- 16-byte/8-word page read buffer
- 64-byte/32-word write buffer
- Extra 128-word sector for security
 - Feature factory locked and identifiable, and customer lockable
- Advanced sector protection function (Solid and Password Protect)
- Latch-up protected to 100mA from -1V to 1.5xVcc
- Low Vcc write inhibit: $V_{cc} \leq VLKO$
- Compatible with JEDEC standard
 - Pinout and software compatible to single power supply Flash
- Deep power down mode

Pseudo SRAM General Features

- Organization: 2M x 16
- Power Supply Voltage: 2.7~3.6V
- Separated I/O power(VccQ) & Core power(Vcc)
- Three state output
- Byte read/write control by UB#/LB#
- Auto-TCSR for power saving
- 8 page mode & DPD

Product Description

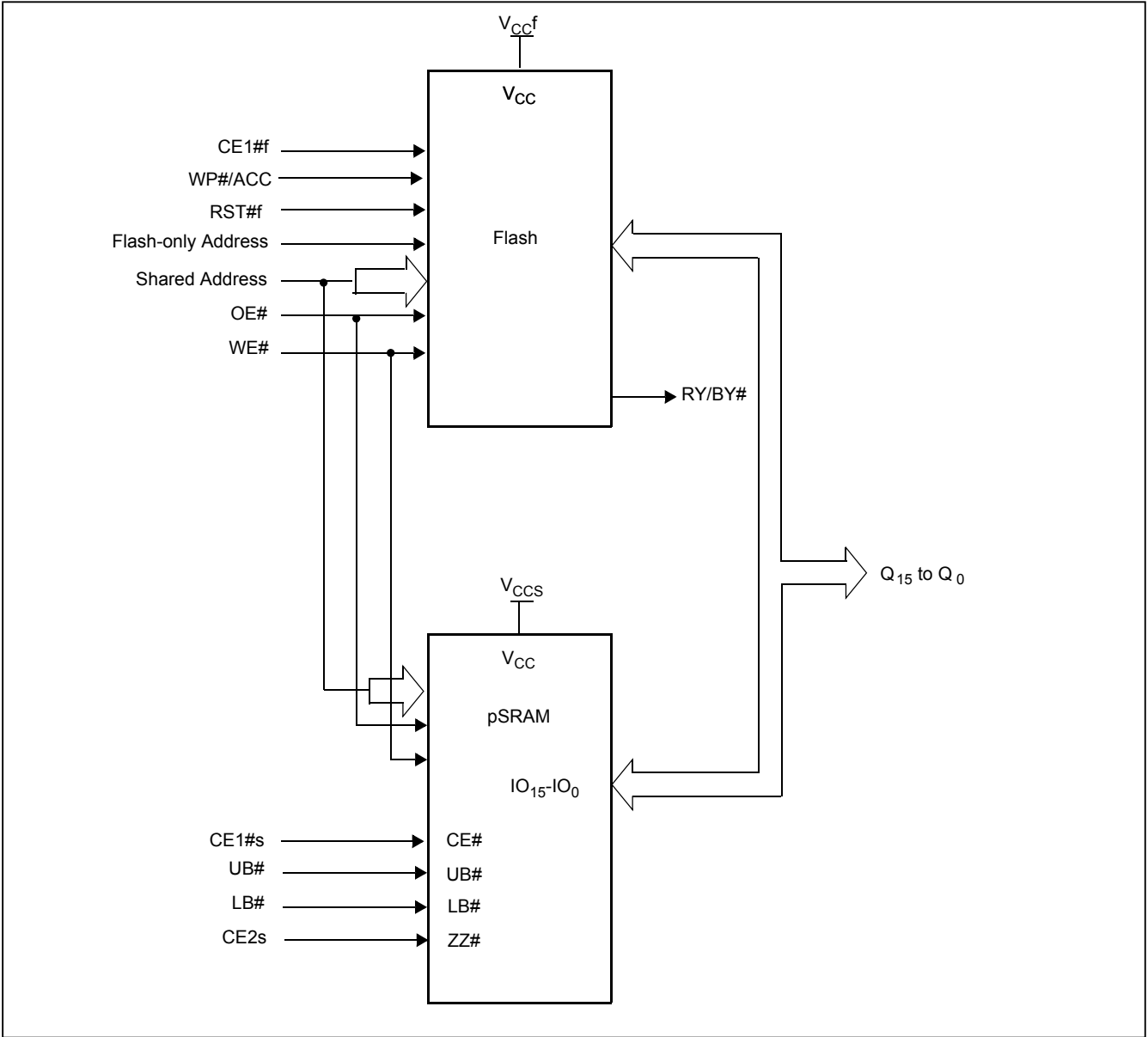
The MX69GL126F product series combine MX29GL128F with pSRAM in a Multi-Chip package. For detailed specifications, please refer to the individual datasheet for MX29GL128F Flash and pSRAM.



Ordering Information

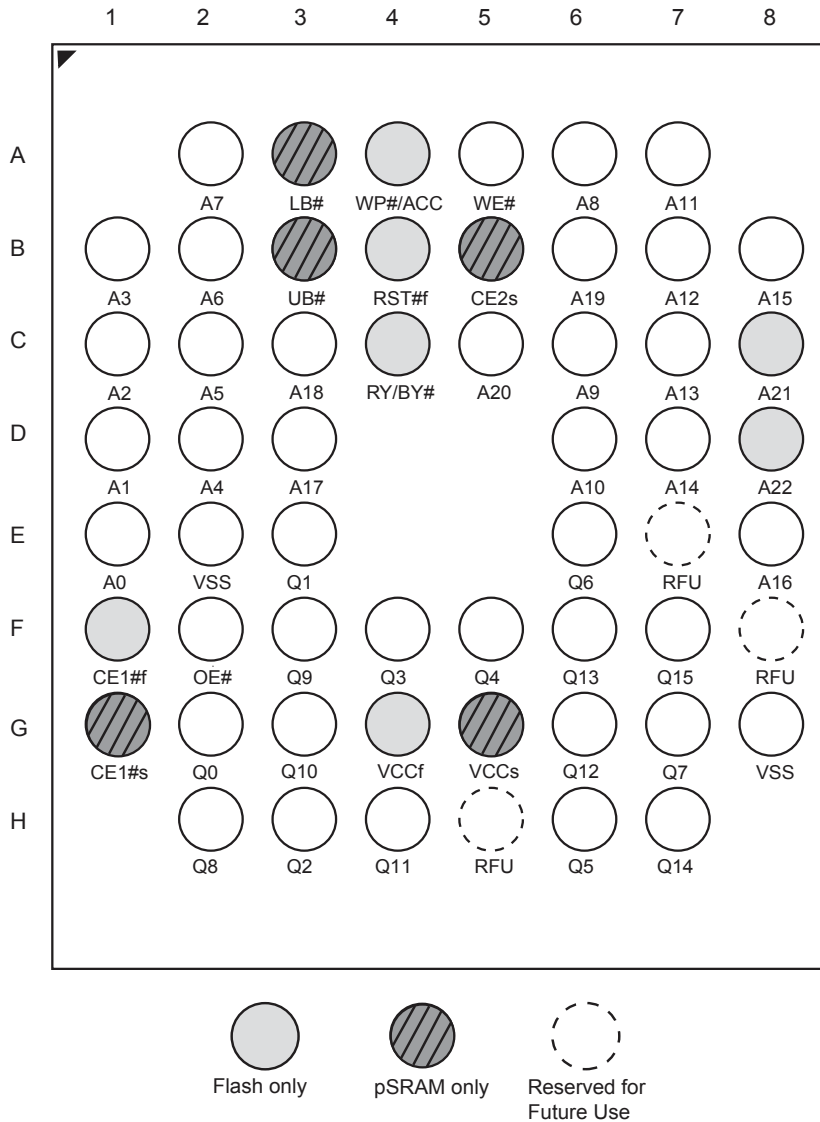
Device	Flash Density	Flash Access Time	pSRAM Density	pSRAM Access Time	Package type	Industrial Grade
MX69GL126FEXGI-90G	128Mb	90	32Mb	70	7x9 56FBGA	V

BLOCK DIAGRAM



PIN CONFIGURATIONS

56-ball Fine-Pitch Ball Grid Array
(Top view through package)



Notes:

1. The address shared by MCP combination as show in the table below:

MCP	Flash-only Addresses	Shared Addresses
MX69GL126FE	A22, A21	A20~A0



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A22~A0	23 Address Inputs for Flash 128Mb (A20~A0 are shared with pSRAM)
Q15~Q0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable Input 1 (Flash)
CE1#s	Chip Enable Input 1 (pSRAM)
CE2s	Chip Enable Input 2 (pSRAM)
OE#	Output Enable Input (Common)
WE#	Write Enable Input (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM)
LB#	Lower Byte Control (pSRAM)
RST#f	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
VCCf	Flash 3.0 volt-only single power supply
VCCs	pSRAM Power Supply
VSS	Device Ground (Common)
RFU	Reserved for Future Use

PART NAME DESCRIPTION

MX 69GL 126 F E XG I - 90 G

OPTION:

G: RoHS Compliant

SPEED:

90: 90ns

TEMPERATURE RANGE:

I: Industrial (-40°C to +85°C)

PACKAGE:

XG: FBGA with 0.4Ball Size, 0.8Ball-Pitch, 1.2mm Total High

pSRAM

E: pSRAM

REVISION:

F

Flash DENSITY & MODE:

126: 128Mb, uniform sector, Lowest Address Sector Protected
(Protection when WP#=VIL), MCP package: 7x9mm, 56Ball-FBGA

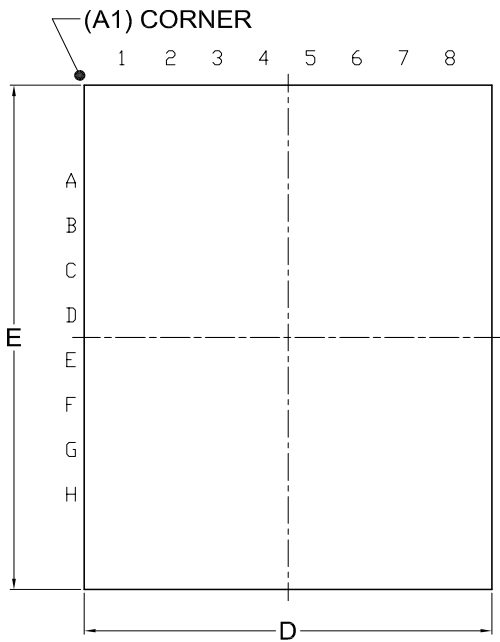
DEVICE:

69GL: Multi-Chip Package
3.0Volt Page Mode Flash Memory and pSRAM

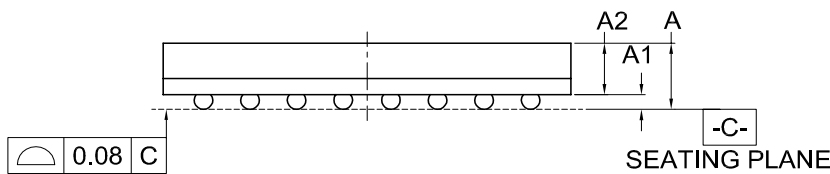
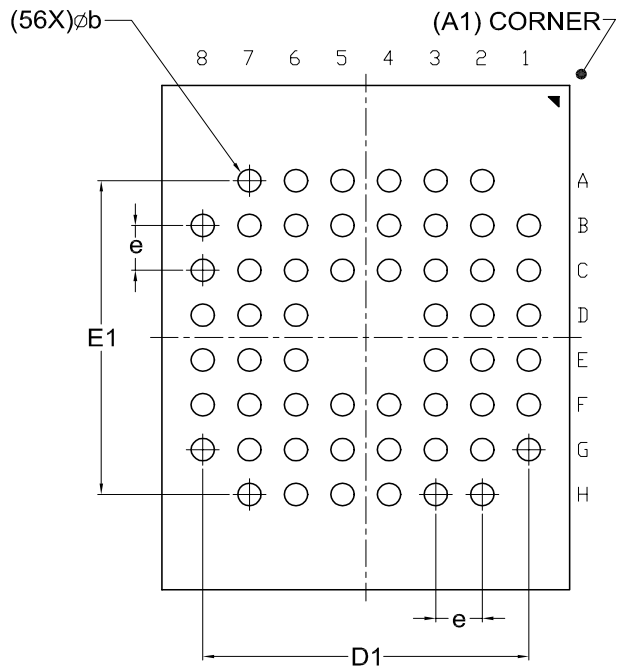
PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 56BALL(7X9X1.2MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW



BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
UNIT										
mm	Min.	---	0.25	0.65	0.35	6.90	---	8.90	---	---
	Nom.	---	0.30	---	0.40	7.00	5.60	9.00	5.60	0.80
	Max.	1.20	0.35	---	0.45	7.10	---	9.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.272	---	0.350	---	---
	Nom.	---	0.012	---	0.016	0.276	0.220	0.354	0.220	0.031
	Max.	0.047	0.014	---	0.018	0.280	---	0.358	---	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4265	1				



REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information" to align with the product status	All	JUL/21/2015



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