

MX69N MCPs

Multiplexed, 1.8V Burst-mode

64 Megabit

(Data Sheet)

Key Features

- *Combine MX29NS-E with pSRAM*
- *56-ball TFBGA Package (6.2x7.7mm)*

MCP FEATURES

- **Power supply voltage of 1.7V to 1.95V**
- **Burst Read: 108 MHz**
- **Package - MCP BGA: 0.5mm ball pitch**
 - 6.2 x 7.7mm, 56 ball
- **Operating Temperature Range**
 - Wireless, -25°C to +85°C
 - Industrial, -40°C to +85°C

Product Description

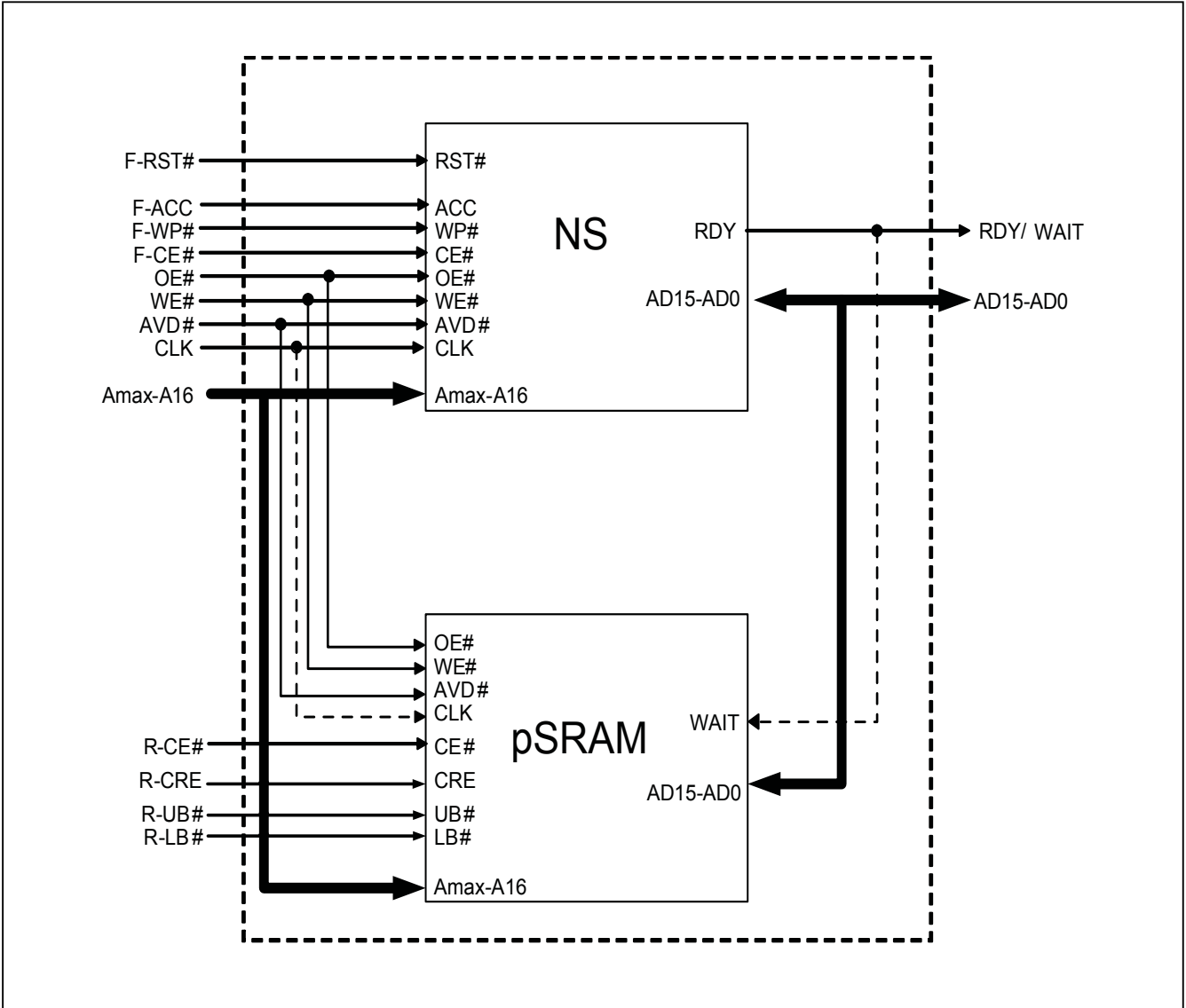
This MX69N-E product series combine MX29NS-E with pSRAM in a Multi-Chip package. For detailed specifications, please refer to the individual datasheet.



Product Selection Guide

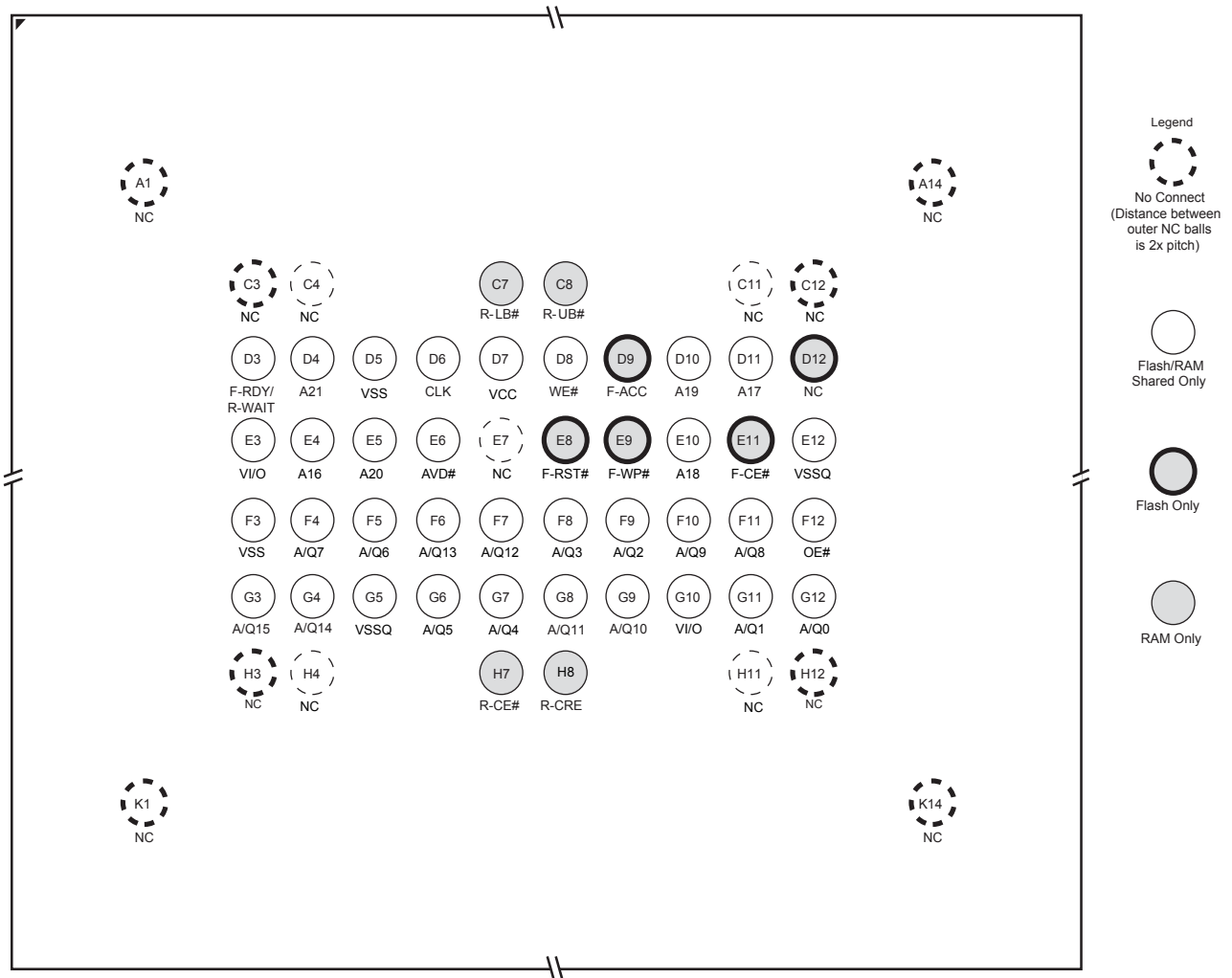
Device	Flash Density	Flash Speed	pSRAM Speed	Package Type
MX69N64E32AXJW	64Mb	108MHz	108MHz	6.2x7.7 56-TFBGA
MX69N64E32AXJI	64Mb	108MHz	108MHz	6.2x7.7 56-TFBGA

BLOCK DIAGRAM



PIN CONFIGURATIONS

**pSRAM Based Pinout, 56-Ball, VFBGA
(Top View, Balls Facing Down)**



Notes

1. Addresses are shared between Flash and RAM depending on the density of the pSRAM.

MCP	Flash-only Addresses	Shared Addresses	Shared AQ Pins
MX69N64E32	A21	A20~A16	AQ15-AQ0

PIN DESCRIPTION

SYMBOL	DESCRIPTION	Flash	RAM
Amax-A16	Address Inputs	V	V
A/Q15~A/Q0	Multiplexed Data Inputs/Outputs	V	V
OE#	Output Enable Input	V	V
WE#	Write Enable Input	V	V
VCC	Device Power Supply (1.70V~1.95V)	V	V
VI/O	Input/Output Power Supply (1.70V~1.95V)	V	V
VSS	Device Ground	V	V
VSSQ	Input/Output Ground	V	V
NC	No Connection	V	V
RDY	Ready output, the status of the Burst Read	V	V
	Refer to configuration register table		
CLK	Clock	V	V
AVD#	Address Valid Data input.	V	V
F-RBST#	Hardware Reset Pin, Active Low	V	
F-WP#	Hardware Write Protect	V	
F-ACC	Programming Acceleration Input	V	
R-CE#	Chip-enable input for pSRAM.		V
F-CE#	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	V	
R-CRE	Control Register Enable (pSRAM).		V
R-UB#	Upper Byte Control (pSRAM).		V
R-LB#	Lower Byte Control (pSRAM).		V

PART NAME DESCRIPTION

MX 69N 64 E 32 A XJ W

TEMPERATURE RANGE:

W: Wireless (-25°C to 85°C)

I: Industrial (-40°C to 85°C)

PACKAGE:

XJ: TFBGA with 56-ball (6.2x7.7mm)

pSRAM Vendor

pSRAM DENSITY :

32: 32Mb

REVISION:

E

Flash DENSITY :

64: 64Mb

DEVICE:

69N : Multi-Chip Product (MCP)

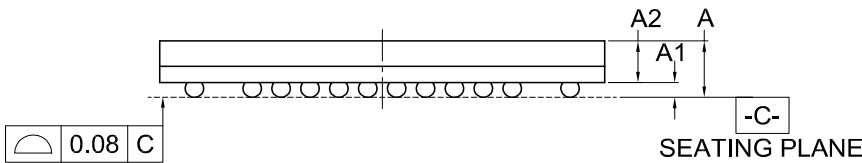
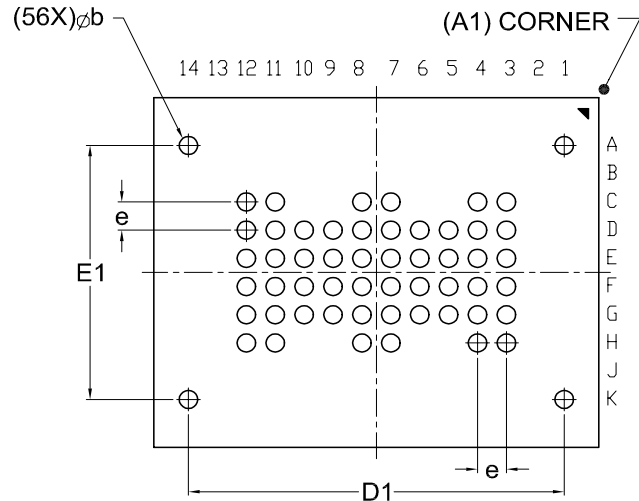
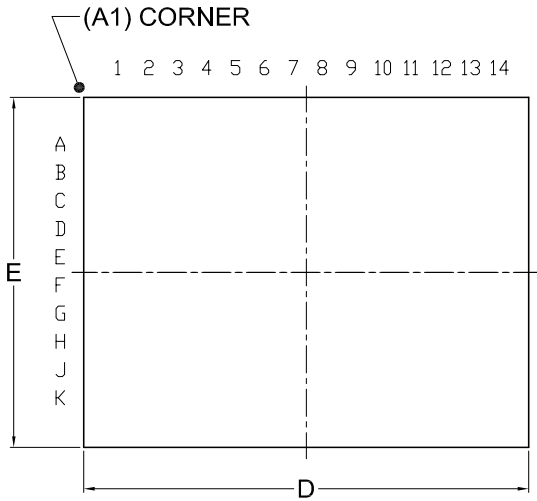
1.8Volt AD-Mux Burst Mode Flash Memory and RAM

PACKAGE INFORMATION

Doc. Title: Package Outline for CSP 56BALL(7.7X6.2X1.2MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)

TOP VIEW

BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	---	---
	Nom.	---	0.21	---	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.20	0.26	---	0.35	7.8	---	6.3	---	---
Inch	Min.	---	0.006	0.026	0.010	0.299	---	0.240	---	---
	Nom.	---	0.008	---	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.047	0.010	---	0.014	0.307	---	0.248	---	---

Dwg. No.	Revision	Reference		
		JEDEC	EIAJ	
6110-4264	1			

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Added MX69N28E64AXJW & MX69N28E64FXJW 2. Modified table-PIN DESCRIPTION	P3,5,7 P6	JAN/18/2011
1.0	1. Removed Advanced Information	P2	MAY/30/2011
1.1	1. Modified Product Selection Guide	P3	MAY/10/2012
1.2	1. Removed 128Mb	All	JUL/22/2013
1.3	1. Modified Pin Configuration	P5	JUL/04/2014
1.4	1. Removed MX69N64E32BXJW 2. Updated speed from 104MHz to 108MHz	P3 P2,3	MAR/20/2015
1.5	1. Removed a key feature: Wireless Grade 2. Added another temperature range: Industrial, -40°C to +85°C 3. Added a new Part No. MX69N64E32AXJI	P1 P2,7 P3	MAY/19/2015



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